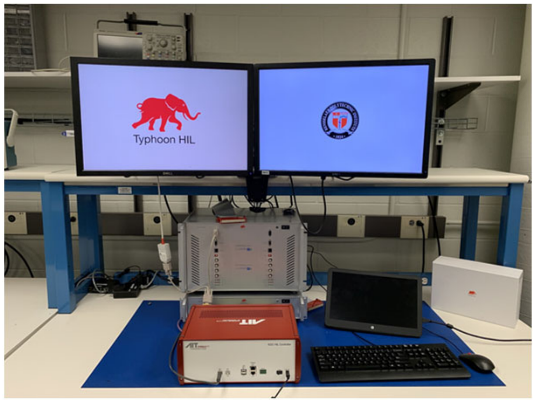


Real-Time Controller Hardware-in-the-Loop Analysis of Ground Fault Overvoltages in Inverter-Based DERs

Prottay M. Adhikari | Luigi Vanfretti

https://alsetlab.github.io/lab/

CIGRE USNC's Grid of the Future, 2021, Providence, RI, 19th October, 2021

cigre United States | National Committee of the United States

Background

Even with all the advances in *power system reliability* through the last few decades, faults and blackouts… still happen.

In terms of fault-statistics, above **75%** of all the faults in the power system are **Single Line to Ground** (SLG) faults.

Thus, synchronous machines have been studied extensively under SLG conditions through the decades.

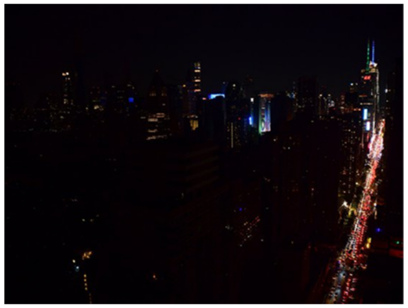


Figure: (left) Pakistan Blackout in Jan, 2021 (right) Manhattan blackout in July 2019

But, as shown in the survey on the right, the global energy portfolio is increasing its share of solar power every year. It is crucial to understand how Solar PV systems behave under SLG conditions, and standardize methodologies to mitigate any prospective issues.

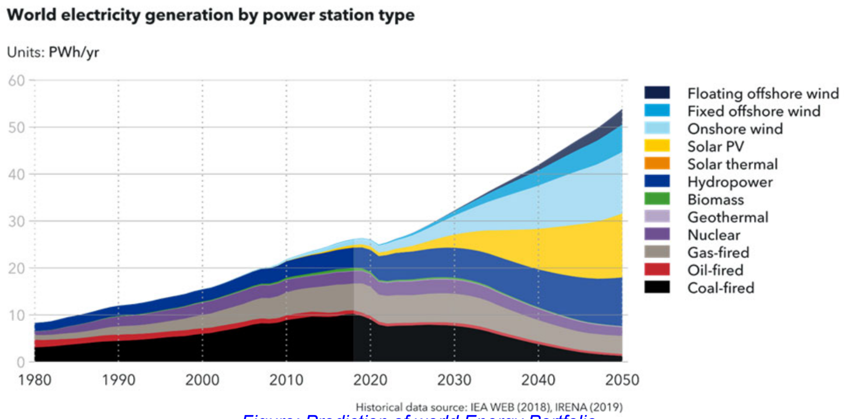


Figure: Prediction of world Energy Portfolio

The theoretical fundamental of this research …

Background

Under SLG faults, synchronous machines are observed to exhibit upto **73%** overvoltages on the unfaulted phases. To mitigate those, IEEE std 62.92 has proposed extensive protection schemes involving grounding strategies.

$$E_a - V_{cn} - E_c = 0; \Rightarrow V_{an} = E\angle 0^\circ - E\angle 120^\circ = \sqrt{3}E\angle 330^\circ$$
$$E_b - V_{bn} - E_c = 0; \Rightarrow V_{bn} = E\angle 240^\circ - E\angle 120^\circ = \sqrt{3}E\angle 270^\circ$$


Figure:Synchronous Machine Installation on the plant-floor

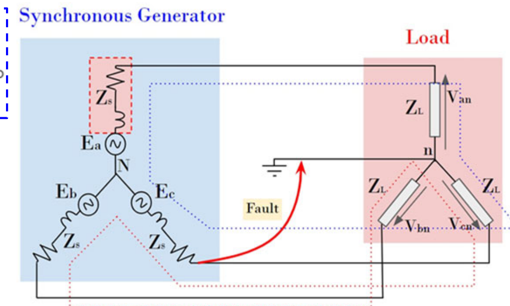


Figure:Synchronous Machine under SLG

Figure: Inverter installation by RWW Engineering, South Africa

But, in modern power grid not all systems are entirely synchronous generator based. IBRs (e.g. Solar PV) are becoming more and more common every passing year.

$$V_{an} = I_a \times Z_a, V_{bn} = I_b \times Z_b$$

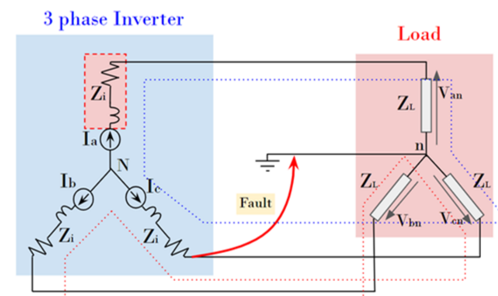


Figure:3 phase inverter under SLG

Motivation

Do IBRs exhibit similar overvoltages when subjected to SLGs? If yes … can *similar* overvoltage mitigation schemes as dictated by IEEE std 62.92 be employed?

These are the questions we are addressing in this research.

Do IBRs models show GFOV under SLG?

Inverters' electrical model is significantly different than that of synchronous generators' - e.g. inverters are **not** possible to model with an internal voltage source.

Inverters' model can be viewed as dependent current sources, as its behavior is driven by controls.
Thus the best way to answer this question is to run perform experiments.

Will standard GFOV mitigation techniques work?

The standard GFOV mitigation techniques target the zero sequence circuit of the system.

We need to run detailed **sequence analysis** of the inverter under SLG to comment on it.

Will std inverter protections help?

Some modern inverters have a Self-protection-overvoltage (SPOV) feature within them, which is standardized in IEEE 1547.2018 std. Will this SPOV feature help the inverters under SLG?

We need to run experiments ***with and without*** the inverter being protected by SPOV feature.

Methodology

To answer these questions, **ALSETLab** designed specific RT-CHIL experiments in collaboration with JEM Engineering, NYSERDA and AIT.

Why Real-time?

To simulate the transient behaviour of the IBRs (e.g. the transient event that lasts 1 sec will be simulated in 1 sec) within the prescribed time in spite of the system-complexity.

Why HIL/CHIL simulation?

To test how an actual controller responds to these transient changes in real time.

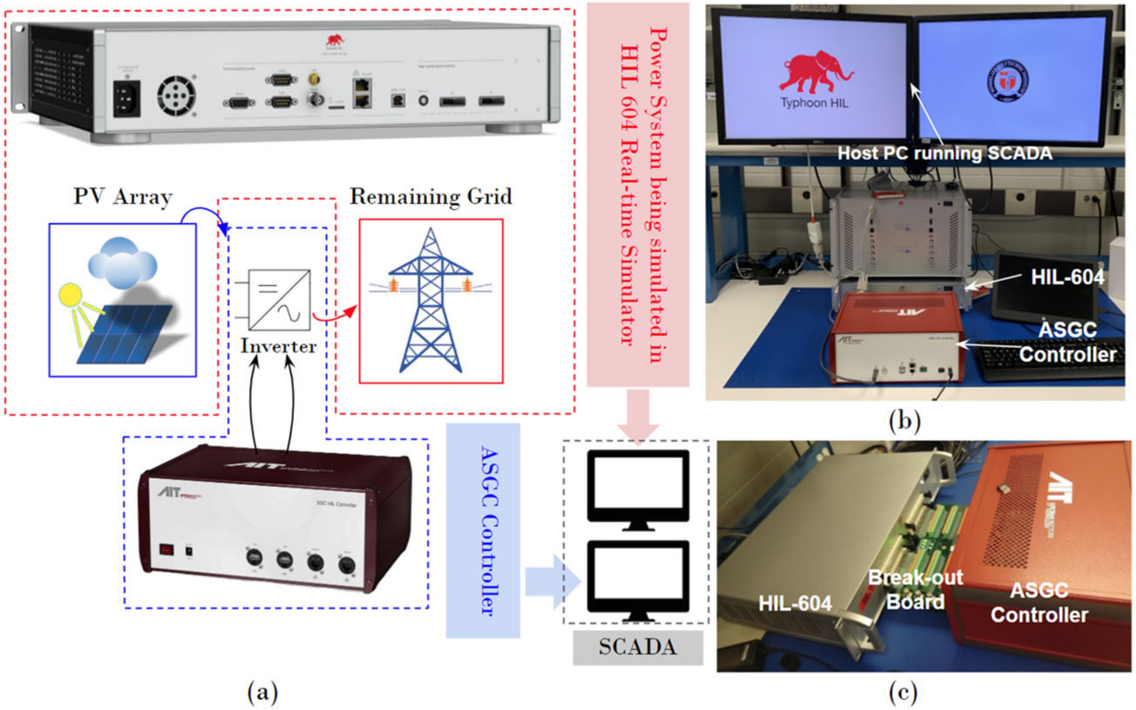


Figure: (a) Pictorial representation of the experimental setup, (b) The physical experimental setup, (c) The interface between ASGC controller and Typhoon HIL 604

System Specifications

Hardware

RT Simulator:

Typhoon HIL 604

ARM Core x 8/ FPGA interfaces

Controller in loop:

ASGC:IEEE 1547 compliant

Communications:

Serial Comm with host

Analog communication

Upto 128 pins between controller and simulator, 5V full-scale analog signal

Digital communication

(upto 64 pins)

Software

HIL Schematic v2020:

Modeling

HIL SCADA

V8+ : Modeling on Simulator

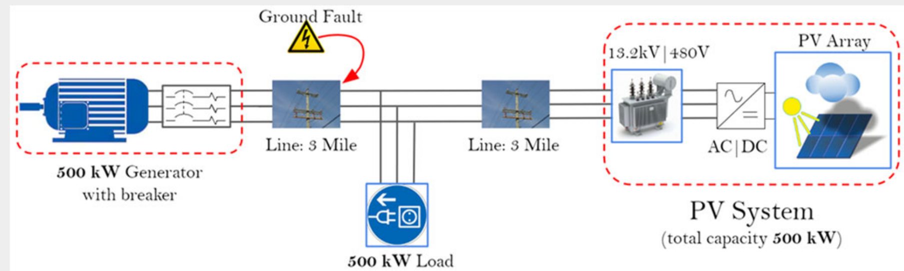
V3.8: Controller

aBoot Flasher:

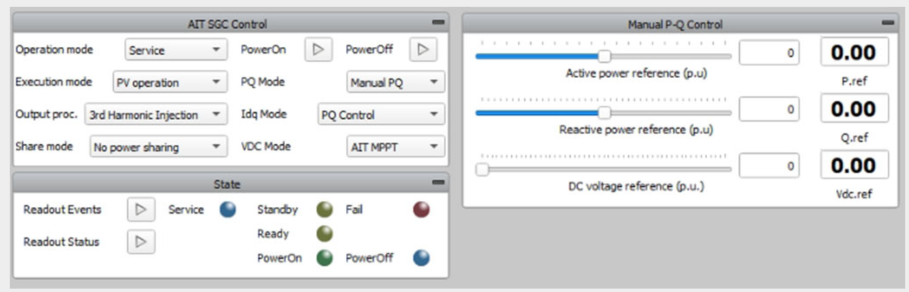
Controller Configuration

Model

Schematic of the System built on simulator:



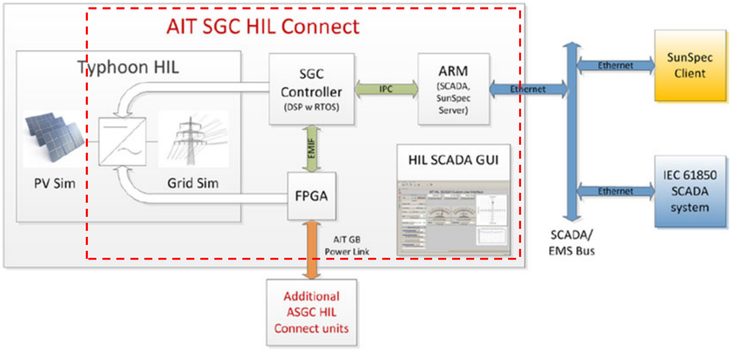
Schematic to interact with the controller:



System Specifications (Focusing on the controller)

- The functional block diagram for the ASGC controller consists of **Typhoon RT-HW** on one end and the **networked interface** (not used in our tests) on the other.

- Following pre-existing test/control infrastructures in the ASGC framework, make experimentation easy
  - PU setting of P/Q allows to vary inverter rated power from a few kWs up to MWs
  - Immediate control available on →
    Connection, **P**, pf, **Q**
  - Built in tests available
    - Volt-Var/Q(U),
    - Frequency-Watt/P(f)
  - Low/High Voltage ride through
  - SunSpec compliant interface
- The controller to computer communication is built upon **serial** communication



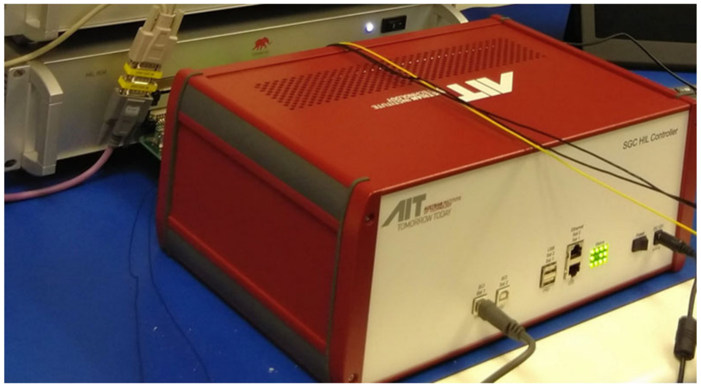


Figure: (a) Block-diagram for the ASGC controller setup (from AIT)
(b) ASGC controller in the ALSET lab connected to HIL 604

System Specifications (Focusing on the controller)

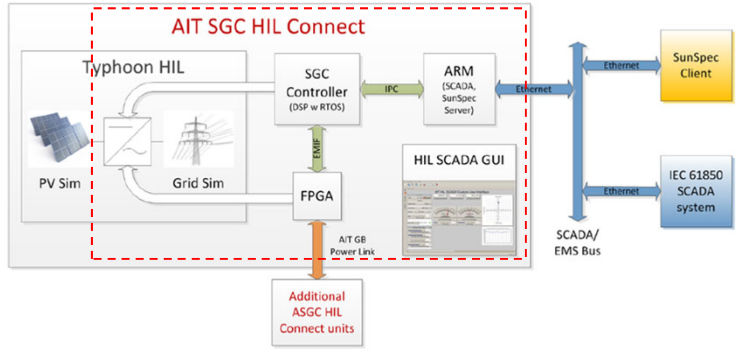
It can do: (as reported)

On the overall power system level

- Managing variability of RES
- Matching supply and demand-
- Ensuring frequency stability
- Ensuring security of supply

On the local distribution level

- Managing voltage profiles
- Avoiding overloading of components
- Transforming passive to active grids
- Integrating PV in Smart Grid concept



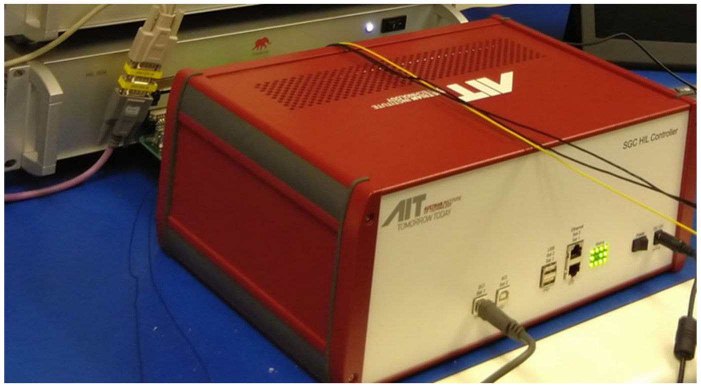


Figure: (a) Block-diagram for the ASGC controller setup (from AIT) (b) ASGC controller in the ALSET lab connected to HIL 604

Design of the experiments

A grid-connected inverter supplying a load of 500 kW is being simulated on the Typhoon HIL 604. This inverter is being controlled by the ASGC controller via the breakout board.

↓

An SLG is introduced via a breaker on the load side.

↓

Make the system run for 35 ms. During this time, huge currents will be fed into the fault by the utility

↓

Disconnect the utility, one phase at a time near the current-zero crossings. Thus, the inverter is left to feed the fault.

↓

Observe the (over)voltages & currents till the inverter eventually disconnects due its own internal protection schemes.

Algorithm 1 Protocol for GFOV Experiments

```
/* SLG Fault Introduction */
if ∠V_a − θ < ϵ then
    if Faulter=1 then
        BKR_F = CLOSE
        State= FLT
        EXIT to next function
    else
        BKR_F = OPEN
else
    Continue Simulation
/* Breaker Opening */
while State=FLT do
    Wait (35 ms) ;
    do in parallel
        if ∠I_a < ϵ then
            BKR_A = OPEN
        if ∠I_b < ϵ then
            BKR_B = OPEN
        if ∠I_c < ϵ then
            BKR_C = OPEN
```

Experiments: the comprehensive list

1. Simulating the inverter GFOV
    a. Facilitating a capacitance Bank

2. Simulating the inverter GFOV with tuned capacitance bank
    a. Vary the generation to load ratio (GLR) and rerun the experiment

3. Run GFOV test with Grounding Transformer
    a. Vary the generation to load ratio (GLR) and rerun the experiment

4. Run sequence analysis on tests described in 2 and 3

5. Load Configuration adjustment
    a. $\triangle$ connected load insertion
    b. Inductive load insertion

6. Analyze the requirement of SPOV protection for IBRs
    a. Overvoltage mitigation
    b. Cumulative overvoltage violation - mitigation

Experimentation continues ...

GFOV testing

Key Points:

- The overvoltage is to be observed between the time utility disconnects and the time the inverter disconnects

- When the fault has occurred and the utility is still connected, it feeds very high currents into the fault.

- Crucially, there's only 2-3 cycles' worth of post-fault data. The frequency of the system was observed to be varying during those cycles. This, makes sequence analysis difficult.

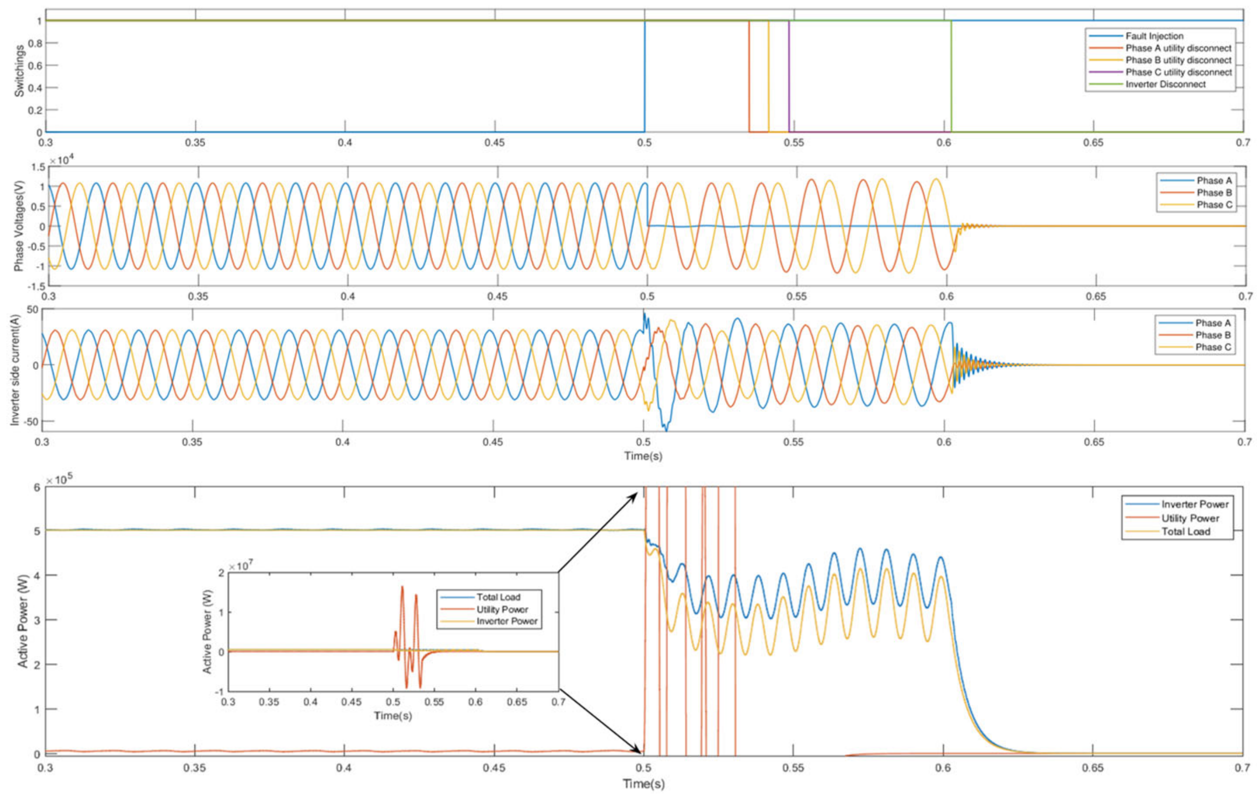


Figure: (a) Switchings (b) Phase Overvoltages (c) Inverter Currents (d) Active power fed into the system - in the GFOV experiment

The need to introduce Capacitance bank

Key Observations:

- The inverter sustains more cycles post-fault
- The post fault overvoltage **is <10%**
- The frequency remains close to 60 Hz till 0.66 sec. This, gives at least 4-5 cycles' data acceptable for sequence analysis.

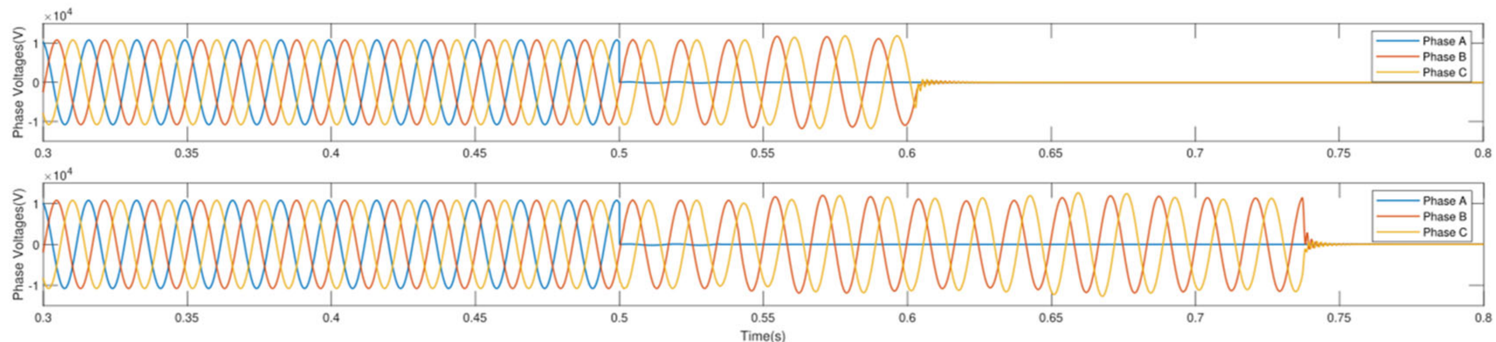


Figure: (above) Phase voltages without a tuned capacitance bank connected across the load (below) Phase voltages with a tuned capacitance bank connected across the load

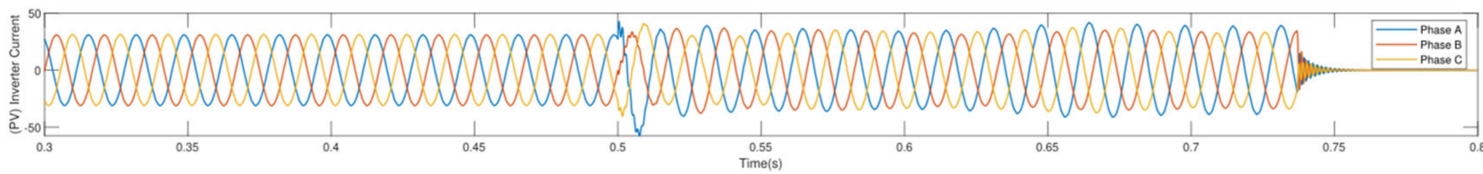


Figure: Three phase inverter currents when the capacitance bank is tuned

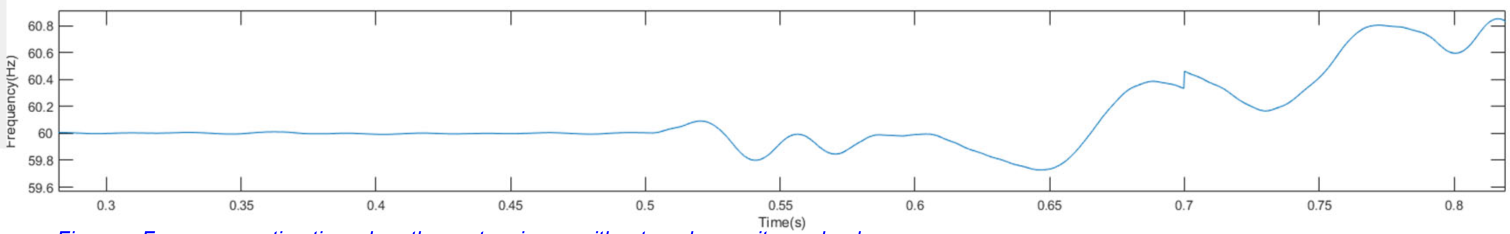


Figure: Frequency estimation when the system is run with a tuned capacitance bank

Overvoltage variation with GLR

Key Observations:

■ The aim in this experiment is to observe the variance of GFOV with GLR (generation to load ratio), and compare it with the variance reported in IEEE std 62.92.6.

■ Two sets of results are presented in the plot on right- one with the controller connected to the system (orange), one without the controller - where the inverter is left to operate on an internal PWM (blue).

■ The overall trend of GFOV v GLR seems to consistent with the IEEE std.

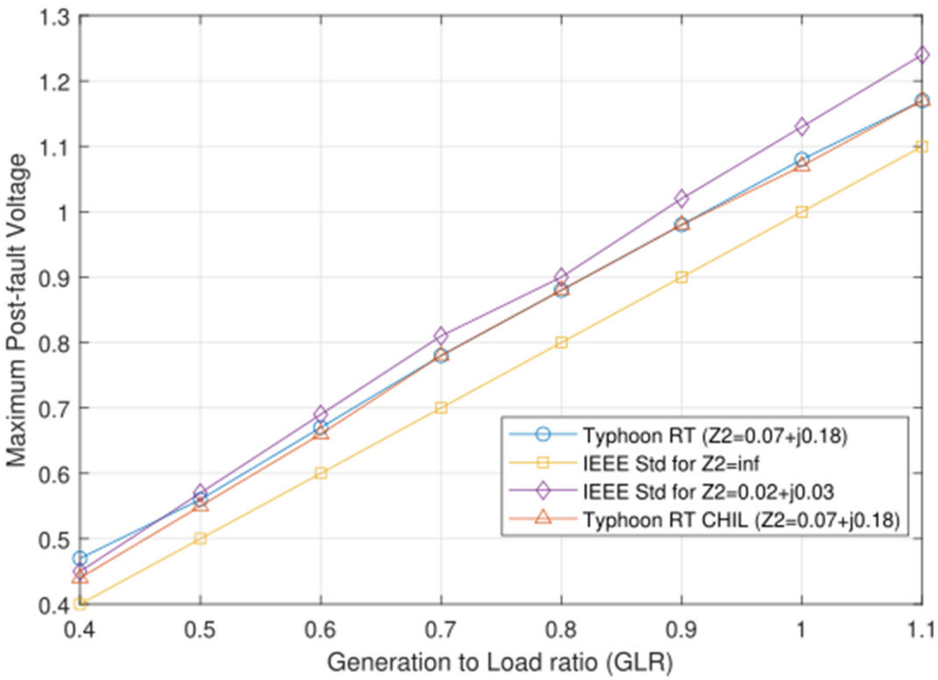


Figure: GFOV vs GLR (Experimental observation and IEEE Std)

Experimentation continues ...

Insertion of a grounding transformer in the system

The phase voltages before and after inserting a 500 kVA GTF in the system.

Sequence components of the currents for the system **with** GTF

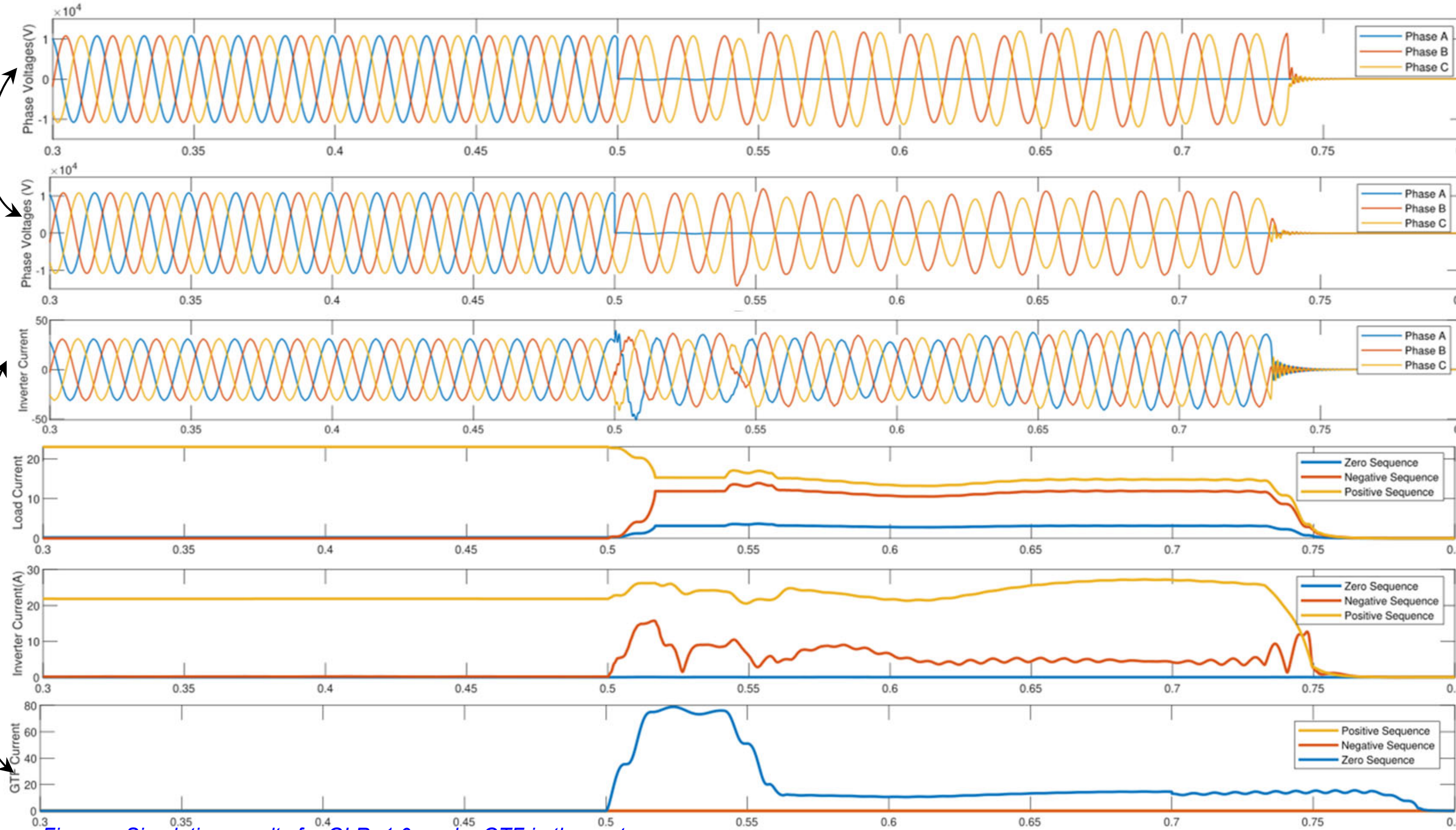


Figure: Simulation results for GLR=1.0, and a GTF in the system

Overvoltage with and without GTF

Table 1: GFOV with and without GTF (Grounding Transformer)

GLR	Over Voltage (Ground Fault No GTF)	Over Voltage (Ground Fault +GTF)	Difference
0.6	0.67	0.62	5%
0.7	0.78	0.73	5%
0.8	0.88	0.84	4%
0.9	0.990	0.935	5.5%
1.0	1.0929	1.071	2.2%
1.1	1.178	1.15	2.8%
1.2	1.296	1.265	3%

■ While the overvoltage is not as severe as it was in synchronous generators, the introduction of GTF **does not** bring a significant improvement.

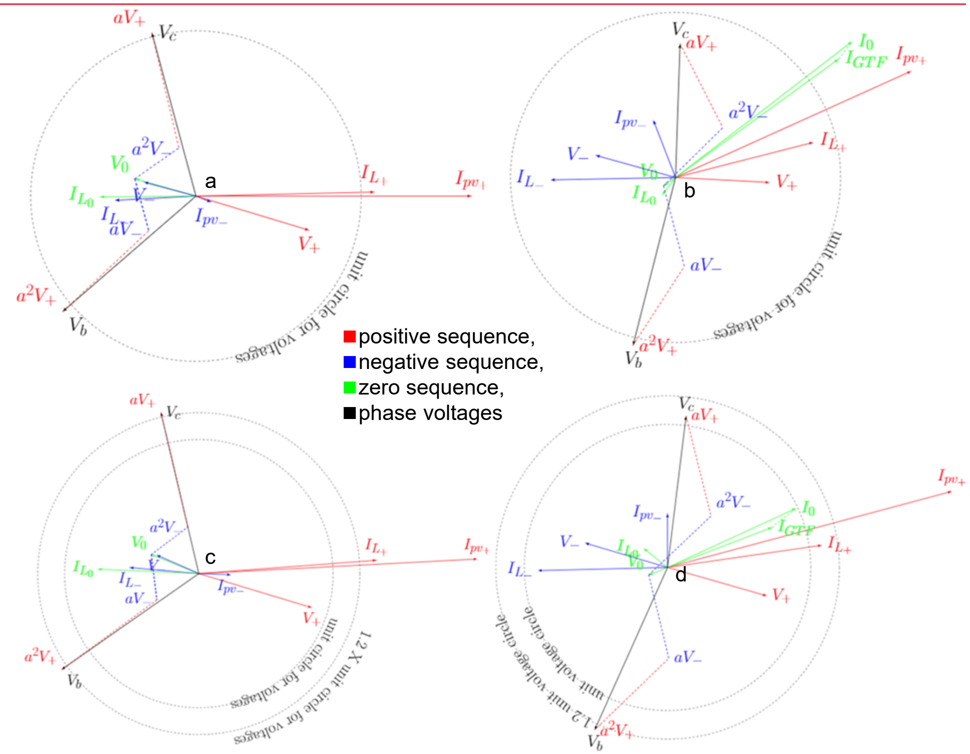


Figure: Phasor Diagrams for (a) GLR=1, no GTF | (b) GLR=1, with GTF | (c) GLR=1.2, no GTF | (d) GLR=1.2, with GTF

Digging deeper into the sequence components of the current ...

Key Observation:

The GTF tampers with the zero sequence circuit and zero sequence currents, but **it increases the negative sequence component** of the voltage. Thus, the GTF can not actually mitigate the overvoltages observed in IBRs under SLG.

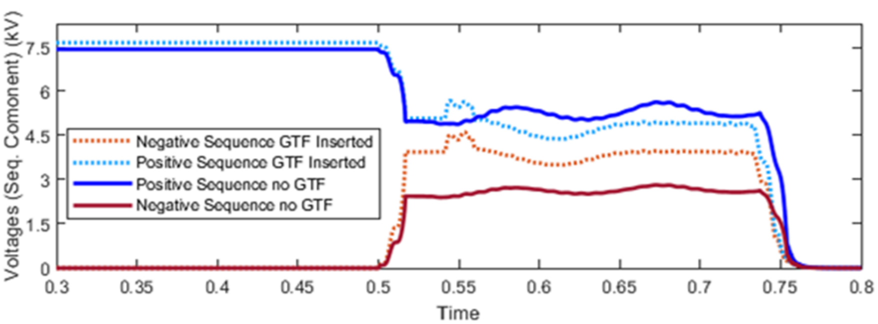


Figure: The sequence components of the voltages with and without the GTF in the system

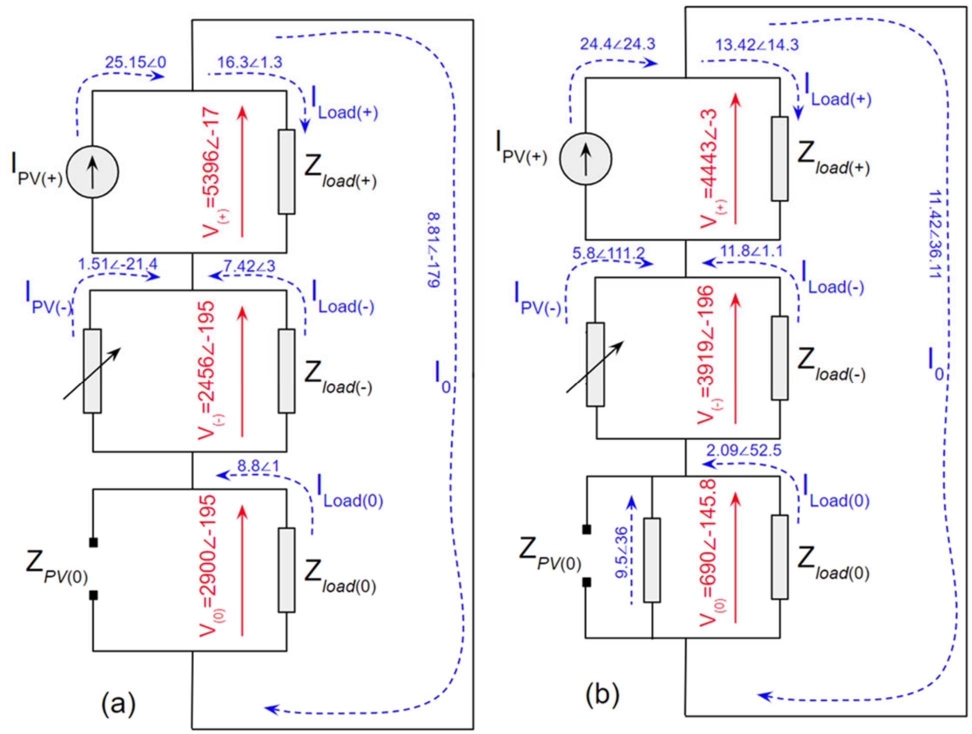


Figure: (a) A snapshot of the sequence diagram of the IBR under SLG without GTF at 0.625s
(b) A snapshot of the sequence diagram of the IBR under SLG with GTF at 0.625s

Experimentation continues ...

Effect of varying load configuration: introducing inductive loads

Table 2: GFOV variation with change in power factor

GLR	Power Factor	Load (kVA)	Overvoltage
1.0	1.0	500	109%
1.0	0.9	556	109%
1.2	1.0	417	130%
1.2	0.9	463	131%

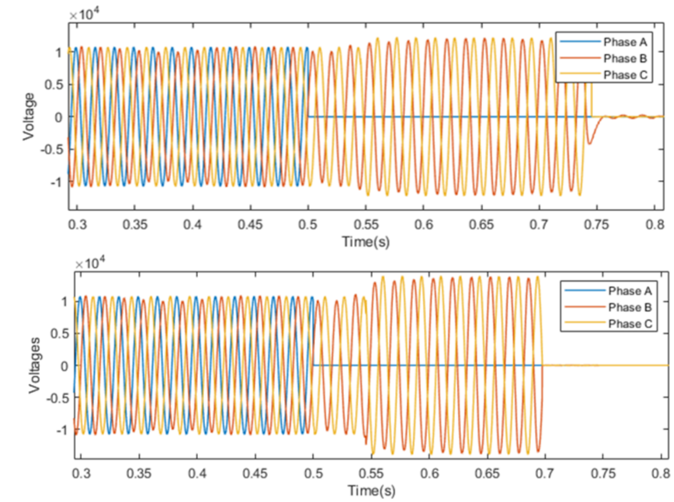


Figure: (a) Overvoltage with GLR=1.0 and pf=0.9
(b) Overvoltage with GLR=1.2

Key Observations:

■ The overvoltage effectively depends on the active power of the load. Thus, the kVA value does **not** affect the GFOV as long as the kW value is kept constant. Thus, the introduction of inductive loads does **not** change the GFOV.

■ For tests with pf=0.9, the effective kW is 500 when GLR=1, which leads to a kVA of 556. When GLR is 1.2, the effective kW=417 - which leads to a kVA of 463.

Effect of varying load configuration: introducing △ connected loads

ALSET lab

Table 3: GFOV variation with △ load injection

Line to ground RMS overvoltage on unfaulted phases	Y = 100%| △=0%	Y = 75%| △=25%	Y = 50%| △=50%	Y = 25%| △=75%
Overvoltage without GTF	1.089	1.19	1.32	1.48
Overvoltage with GTF	1.05	1.07	1.07	No good observations

Key Observations:

- The overvoltage is more prominent when the share of △ connected loads increase.
- GTFs **may be** effective in *reducing* those *overvoltages*.

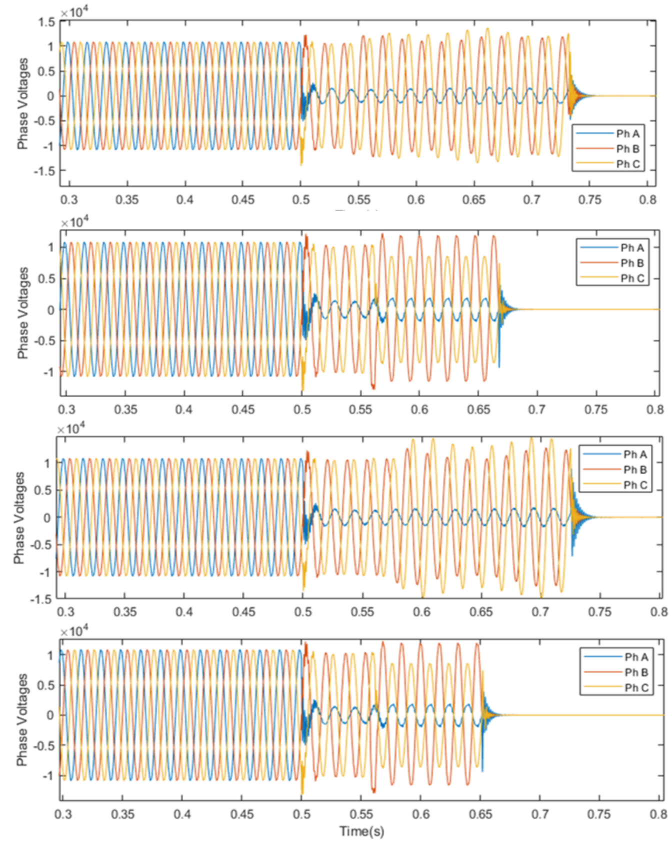


Figure: (a) Overvoltage @ 25% △ load, (b) Overvoltage @ 25% △ load with GTF, (c) Overvoltage @ 50% △ load, (d) Overvoltage @ 50% △ load with GTF

Conclusions

- While synchronous machines can give rise to a **73%** overvoltage under SLG, the overvoltage for IBRs under SLG is of the magnitude of **~10%** when the inverter capacity matches the load demand.This overvoltage **increases** proportionally while the generation-to-load-ratio (**GLR**) is increased.

- Conventional grounding equipments like grounding transformers **can not** mitigate these overvoltages. They only improve the overvoltage by upto **3-5%**. For Y connected loads, grounding transformers reduce the zero sequence voltage, but they increase the negative sequence current- thus, they can't mitigate the overvoltage entirely.

- If △ connected loads are introduced in the system, the overvoltage tend to increase. The GTF is quite **effective** in mitigating the maximum overvoltage.

Rensselaer

why not change the world?®