21, rue d'Artois, F-75008 PARIS
http: //www.cigre.org

CIGRE US National Committee
2021 Grid of the Future Symposium

Hardware-in-the-loop Testing of Overcurrent Protection in a Substation Power System with PV Generation

B. WANG
Virginia Polytechnic
USA

R. LIU, G. ALVAREZ, M. TILL
Dominion Energy
USA

SUMMARY

With increasing penetration of Distributed Energy Resources (DER) such as utility-scaled PV facilities, power system fault characteristics are likely to underdo some major changes, which is likely to increase the complexity of protection schemes design. To prevent incorrect relay operation conditions, it is necessary to test and validate digital relay devices prior to installing them in the field. Hardware-in-the-loop (HIL) simulation is a powerful tool for relay hardware testing which allows providing accurate electromagnetic dynamic behaviors without damaging any physical power equipment. The Dominion Energy Training Center is using an HIL simulator system to provide training programs for technicians in an effort to reduce human performance errors, such as CT tap and polarity errors. In this paper, a Dominion Energy virtual substation with a high PV penetration level was implemented in a RTDS platform, a hardware-in-the-loop simulation was performed to test the protective relay schemes. Simulation results under different fault locations in substation system are shown, which verifies the reliable operation of SEL-451 relay.

KEYWORDS

Hardware-in-the-loop, RTDS, Power system protection, SEL-451 protective relay, Photovoltaic

biqiw@vt.edu

I. INTRODUCTION

Digital microcontroller-based protective relay devices play a significant role in maintaining the power grid, making it reliable and secure against abnormal conditions. Overcurrent relay is the most extensively applied element to prevent undesirable damage from excessive currents [1][2]. The Schweitzer Engineering Laboratories (SEL) relay SEL-451 is able to monitor a power system utilizing voltage and current signals from CTs and PTs, and then send trip signals to circuit breakers with interior protection functions under short-circuit faults to minimize the extent of the outage. Incorrect relay settings are likely to cause false tripping or even bypassing fault conditions, which could lead to a system catastrophe [1]. To ensure the proper relay operation and avoid hazardous unpredictable behavior, it is essential to assess and test the protective relay devices' performance prior to installing them in the field and interconnecting them with the power system [1][3][4].

Real-time Hardware-in-the-loop (HIL) simulation is a relatively mature methodology for electrical apparatus testing. It has been widely used in engineering design, especially in relay equipment validation, power electronics design, the automotive industry, and control [5]. HIL simulation refers to a combination of "rest of system" real-time computer simulation and actual physical components that are connected to the simulation. This incorporates the merits of both real-time simulation and real hardware testing, allowing researchers to test and debug the hardware components under various scenarios in an environment that is close to actual operation [3][4][6][7].

In the case of relay devices' performance validation, the HIL technique places all potentially dangerous power equipment into a real-time simulation, then interfaces with the actual relay device, which mimics the real system and allows the testing of a full range of operation conditions without the risk of damaging any power hardware. Thus, HIL simulation provides an attractive trade-off between low testbed cost, good test fidelity, and excellent test coverage [6].

In recent years, little of the literature has focused on HIL testing of SEL relay devices. [1] validated a proposed HIL model using the overcurrent protection feature in the SEL-487E on the OPAL-RT platform. [5] validated the relay model for the SEL-351S directional over-current relay by performing an HIL test on a Shipboard Power System (SPS). [8] verified the protection scheme using the SEL-411L group setting function on a 154-kV SFCL system in South Korea, based on an HIL simulation in RTDS. [9] tested physical relays SEL-421 and SEL-351A in various cyber-physical system testbeds using the OPAL-RT. [10] presented a real-time HIL implementation for power systems protection, which was carried out on the OPAL-RT platform, based on MATLAB & Simulink and using the SEL-351 protection system. The HIL relay testing in Dominion Energy's Blackstart plan was performed in [11] by deploying RTDS, amplifier and actual SEL 421 relays.

A newer, much more flexible simulator system is utilized in Dominion Energy's Power Delivery Training Center, which allows common system faults and errors to be replicated for

demonstration and troubleshooting purposes without re-writing the circuit. This paper focuses on HIL testing of the SEL-451 relay tripping logic in a virtual substation in the Training Center, with utility-scaled PV generation. The real-time HIL simulation was implemented in the RTDS platform, and results from RTDS could be used to benchmark HIL simulation in OPAL-RT.

Section II of this paper gives a brief introduction to substation topology and PV converter control. Section III presents the details of the SEL-451 main tripping logic. HIL simulation results under different fault scenarios are discussed in Section IV. Finally, in Section V, conclusions are drawn, and future work is outlined.

II. SUBSTATION SYSTEM MODEL

a. Virtual Substation Topology

The topology of the Dominion Energy Training Center virtual substation is shown in Figure 1, where a 34.5 kV bus was supplied by an equivalent model of the transmission system through a step-down transformer and two PV facilities. The power rating of the inverters are 10 MW and 21 MW, respectively. The load power factor was set as 0.99.

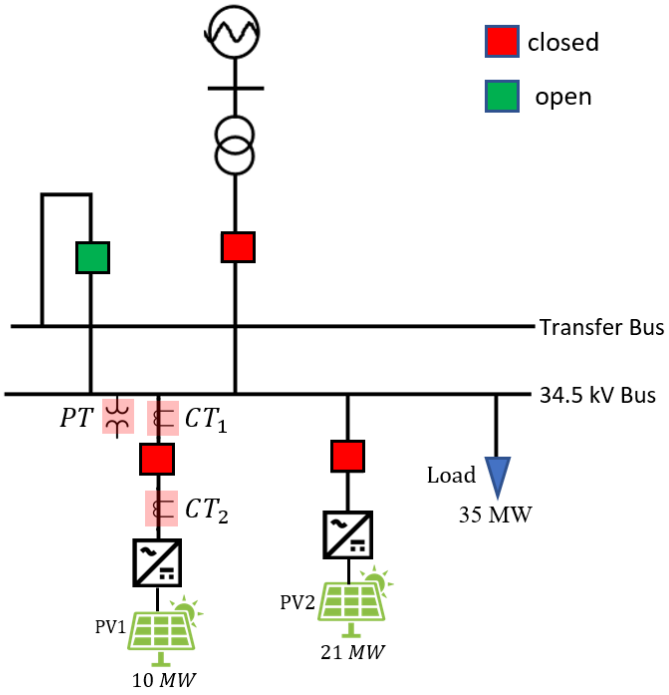

Figure 1. HIL testing platform of virtual substation model

Under normal operating conditions, PV1 is interconnected to the 34.5 kV bus through a circuit breaker in closed status. Our HIL testing focused on the relay scheme of the circuit breaker that interconnects PV1 to the 34.5 kV bus. Two Current Transformers (CTs) were installed, one at

the bus side of the circuit breaker and another at the line side, to provide current measurements for relay. A Potential Transformer (PT) was installed on the 34.5 kV bus to provide bus voltage signal. The circuit breaker between CT_1 and CT_2 will be opened under certain fault scenarios to isolate the faulted part from rest of the substation system.

b. PV inverter Control Scheme

Error! Reference source not found. presents the PV facilities' topology and the inverter's control scheme, where the PV array is integrated to the substation power grid through a three-phase, half-bridge inverter and a DC-link capacitor. A two-stage LCL filter was applied to filter out the switching ripples and harmonics; the leakage inductor of the step-up transformer plays the role of grid side inductor L_2. The LCL filter design methodology can be found in [13]. In both RTDS and the HYPERSIM model, the inverter's average model is deployed for a faster simulation in time domain, while still maintaining an accurate enough converter dynamic. The main parameters of the inverter average model for PV1 and PV2 are shown in Table I.

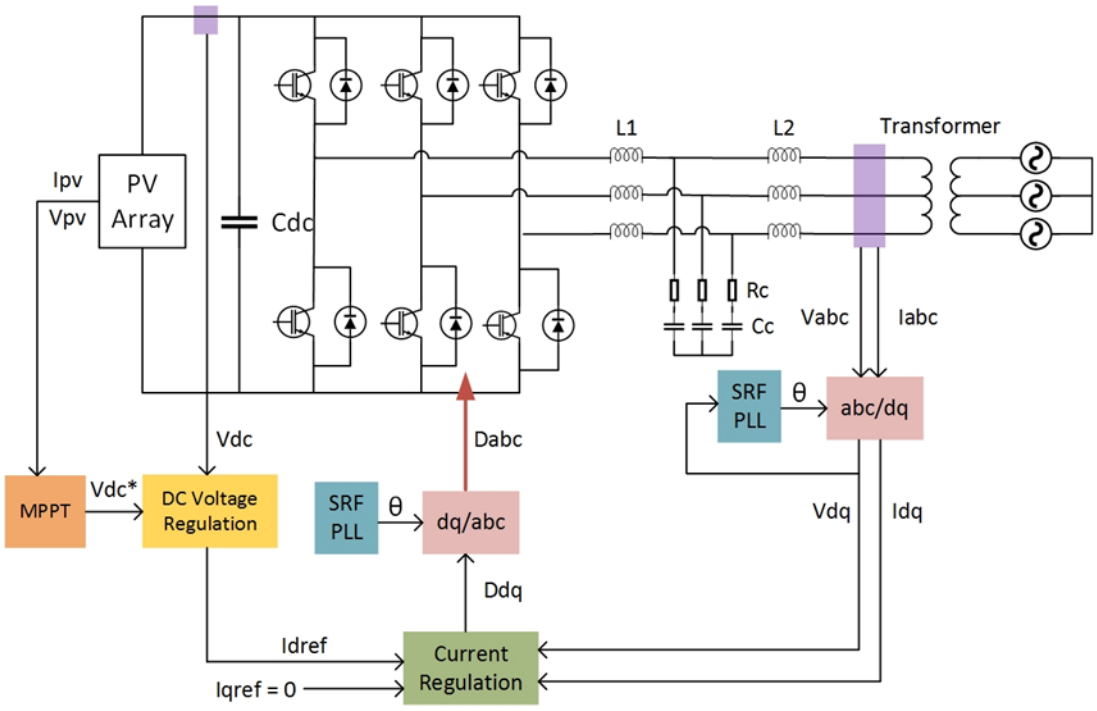

Figure 2. PV inverter topology and control scheme

Table 1. Main parameters of PV inverter average model

PARAMETER	VALUE
Rated DC Voltage	1.2 kV
Rated Inverter Apparent Power	10 MW/21 MW
Rated AC Voltage (line-to-line)	480 V
Sun irradiance	1000 W/m^2

Cell temperature	25 ℃
PV Module Open circuit voltage (V_oc)	21.7 V
PV Module Short-circuit current (I_sc)	3.35 A
PV Module Maximum power point voltage (V_mpp)	17.4 V
PV Module Maximum power point current (I_mpp)	3.05 A
DC-link Capacitance (C_dc)	5000 μF
Inverter side inductance (L_1)	19.6 μH / 9.33 μH
LCL filter capacitance (C_c)	2500 μF

The Lambert function approximation technique was deployed as the Maximum Power Point Tracking algorithm to generate a reference value for the DC voltage regulation loop. This ensured that the PV array was operating at its maximum output electrical power. The outer loop controller, the block diagram of which is shown in **Error! Reference source not found.**(b), was able to regulate the DC-link voltage and produce the inverter output current reference on d axis. Also, the PV inverter was operating at unity power-factor mode, which gives no reactive power injection to grid and thus forced the I_{qref} value to be zero. Current references on both the d and q axis were provided to the inner AC current loop, and duty cycles were generated for the average model simulation after being transformed to abc coordinates. The inner current loop control diagram is shown in **Error! Reference source not found.**(c), where $L = L_1 + L_2$. The capacitor in filter was ignored for control coupling terms. A saturation limiter was imposed on current reference values, which limited the inverter current reference magnitude under 1.5 times of rated value.

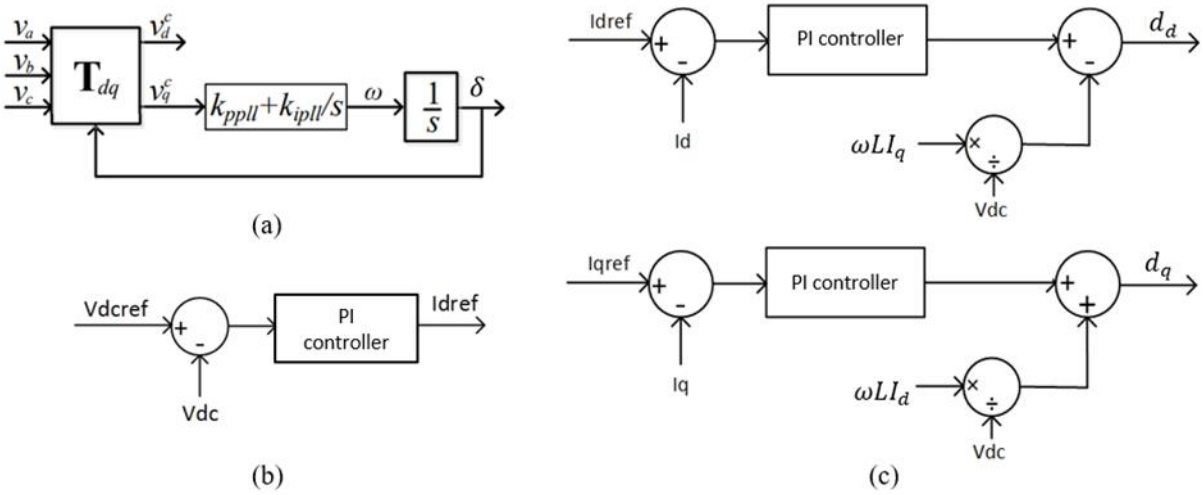

Figure 3. PV inverter control loop diagram (a) PLL (b) DC regulation loop (c) Current loop

III. SEL 451 RELAY TRIPPING LOGIC

a. Overcurrent Relay

Overcurrent relay is one of the most widely used relay schemes in a transmission and distribution network. The main tripping logic for the circuit breaker (as indicated in Figure 1) was overcurrent protection, implemented in the relay hardware with SEL-451 relay protection functions. Both the instantaneous overcurrent protection element (50) and the inverse-time overcurrent element (51) were included. The tripping of all overcurrent function was based on the current measurements sent from the bus side CT. Under normal operation, the rated value of CT second-side current RMS was 0.418 Amps.

A tripping signal from the instantaneous overcurrent element is generated if the analog current signal received on the SEL-451 relay device side is greater than the preset threshold. In our case, the 50P1 element sent out the tripping logic immediately when the maximum RMS value of three-phase current signal from the bus-side CT exceeded 12.83 Amps.

The tripping time of the inverse-time overcurrent relay was developed using the inverse-time curve standard from IEEE C37.112-2018, *IEEE Standard for Inverse-Time Characteristics Equations for Overcurrent Relays*. The relay operating time can be expressed by:

$$T_p = TD\left(\frac{A}{(\frac{I}{I_s})^p - 1} + B\right) \quad (1)$$

where TD is time dial setting, I_s is the pickup current, and I is the actual current. According to the U.S. standards [12], the inverse-time characteristic curve can be categorized into several different types by the degree of curve inversity. The very inverse curve (U3) was applied in this protection scheme. The inverse-time curve parameters could be given as

$$T_p = TD\left(\frac{3.88}{(\frac{I}{I_s})^2 - 1} + 0.0963\right) \quad (2)$$

The inverse-time overcurrent element operates with the time delay given in (3) if the RMS current received exceeds the 1.8 A threshold. Protection against single-phase faults is provided by zero sequence current inverse-time and zero sequence instantaneous overcurrent elements.

b. Circuit Breaker Internal Fault Detection

Detection of a circuit breaker fault is based on current measurement results from both the bus-side and PV-side CT. Under normal operation, the two CTs will sense currents with the same magnitude and different direction. During a circuit breaker internal fault, the fault current increases at both sides of the circuit breaker. However, the bus side fault current will be much larger than the PV side, due to the 1.5 p.u. saturation limit imposed on a converter current control loop. The detection methodology is a logic combination of overcurrent elements from both CTs; the logic diagram is shown in Figure 4. When there is only bus side CT instantaneous

overcurrent element act, the tripping signal is generated from detection logic to trip circuit breaker.

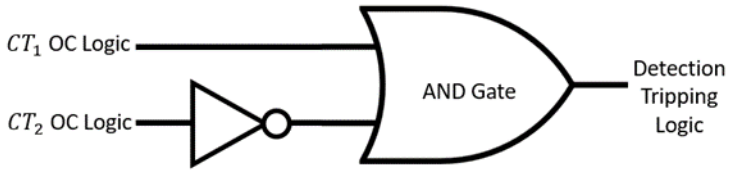

Figure 4. Circuit breaker internal fault detection logic

IV. HIL Simulation Results

The architecture of the relay testbed in the RTDS HIL platform is shown in Figure 2. During the real-time simulation, two sets of three-phase current measurements and one set of three-phase voltage measurements were taken at the secondary side of the PT and CTs and sent to the Giga-Transceiver Analogue Output card, which provided analog voltage and current signals to the SEL-451 relay device through the amplifier. The SEL-451 relay was able to monitor the substation model and generate a tripping signal under various fault scenarios. The digital control signal was sent to RTDS through the Gigabit-Transceiver Front Panel Interface (GTFPI) to trip the circuit breaker between PV1 and the 34.5 kV bus.

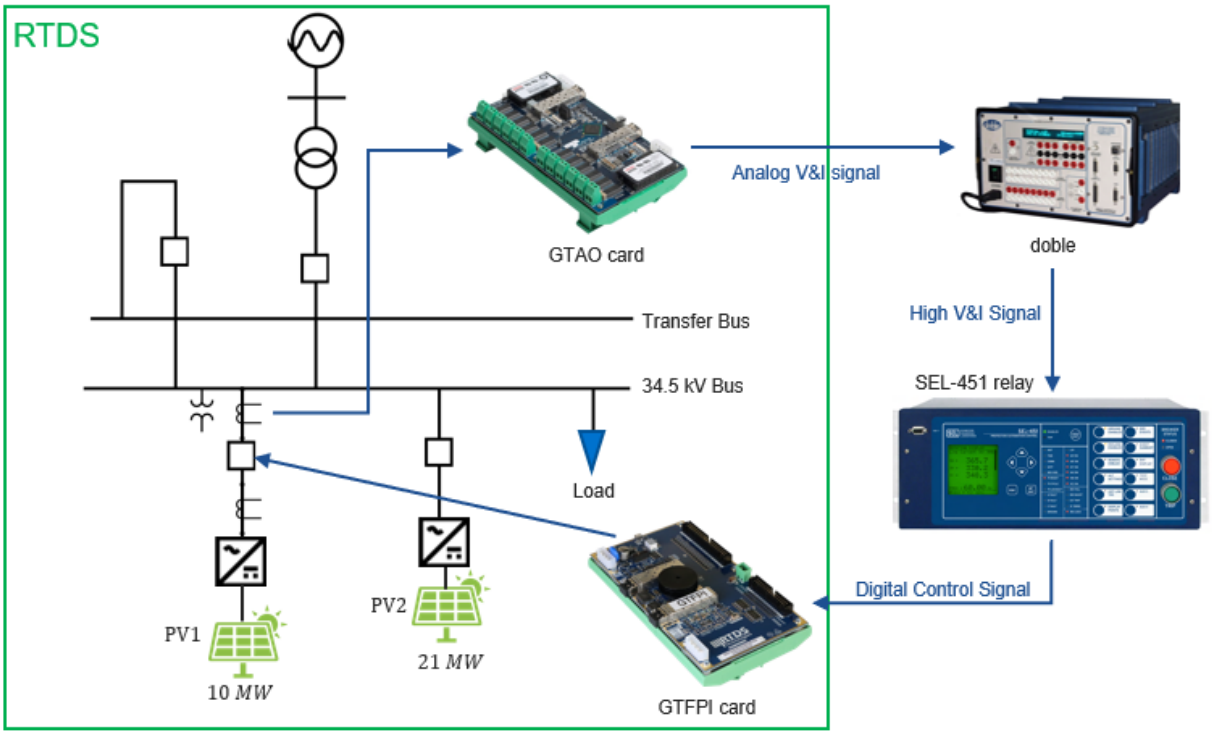

Figure 2. HIL testing platform of virtual substation model

Several fault scenarios in different locations was tested to verify the reliability of the SEL-451 relay tripping logic discussed in Section III. It was assumed that the relay scheme programmed into the relay device would be able to detect the fault occurrence and trip the circuit breaker correctly under different scenarios. Three-phase-to-ground transient faults were applied at the PV inverter terminal, between CT_1 and CT_2, and also on the 34.5 kV bus, in order to emulate a PV internal fault, a circuit breaker internal fault and a bus fault. During a three-phase fault event, fault current on the relay installation location rose to 5.3 kA, which is 31.67 times the rated PV output current. The fault duration was set as 0.3 s.

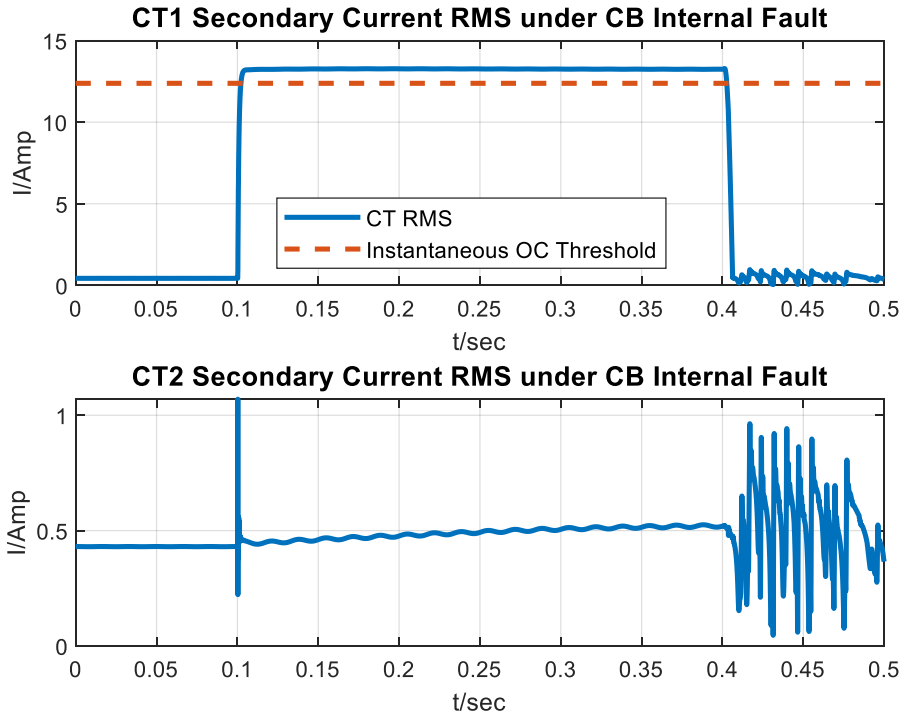

Figure 3. CT current RMS under PV internal fault

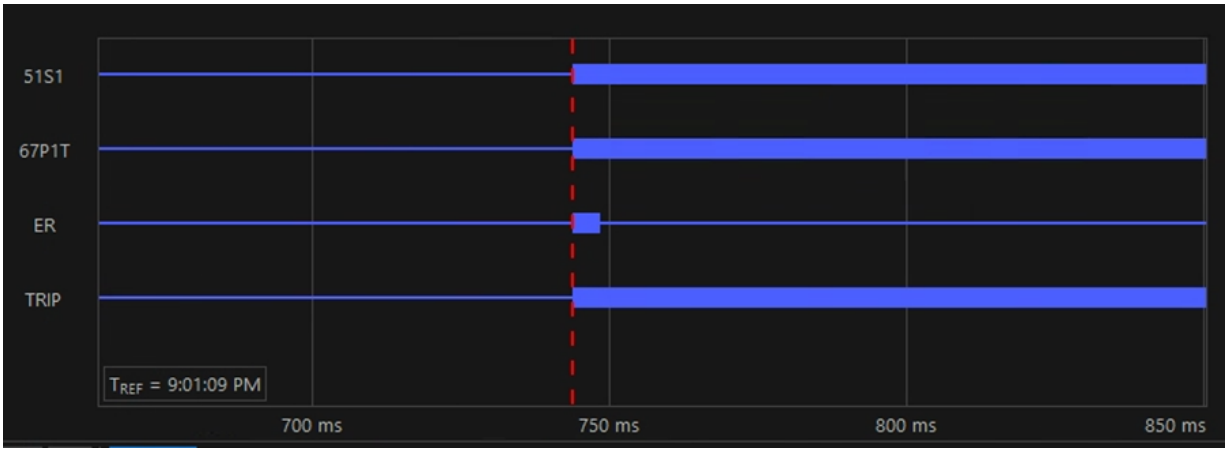

Figure 4. Relay function tripping signals under a PV internal fault

When a fault occurs inside a PV facility, the fault current will flow from the bus to the fault location, and CT_1 and CT_2 will sense fault current with the same magnitude and opposite direction. The response of relay elements will be recorded by the SEL-451 device during a fault event, which will instantly generate a tripping signal to open the circuit breaker when the fault occurs. The CT current RMS fault response under a three-phase-to-ground PV internal fault is shown in Figure 6. The current RMS on both CTs increased to a high level--close to 13.25 during the fault. The secondary side current on the bus-side CT immediately exceeded the threshold of 12.38 A. Figure 7 indicates the operation of relay functions during a PV internal fault, where the thicker line represents the relay function that became a logic 1 and trip. It can be seen that the instantaneous overcurrent element 67P1T operated immediately when the CT_1 measurement signal exceeded threshold.

For a circuit breaker internal fault, the fault current magnitude measured on CT_1 and CT_2 will differ greatly. As shown in Figure 3, the current RMS on the bus-side CT rises over the instantaneous threshold of 12.38 A after a very short time delay of the fault occurrence, while the PV side fault current only increases slightly due to the current loop saturation limit. It stays below the inverse-time overcurrent threshold of 1.8 A. According to the circuit breaker's internal fault detection methodology illustrated in **Error! Reference source not found.**, overcurrent is only detected on the bus-side CT, and the circuit breaker internal fault detection element PSV14 will trip. As indicated by Figure 6, during a circuit breaker internal fault, the instantaneous overcurrent element 67P1T and the circuit breaker internal fault detection element PSV14 will both operate immediately, which generates a digital control signal to trip the circuit breaker.

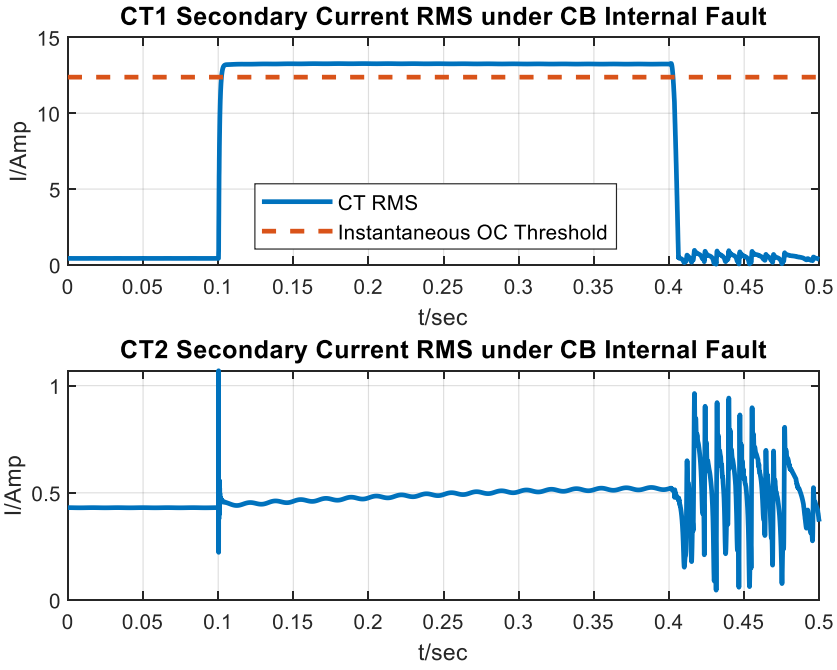

Figure 5. CT current RMS under a circuit breaker internal fault

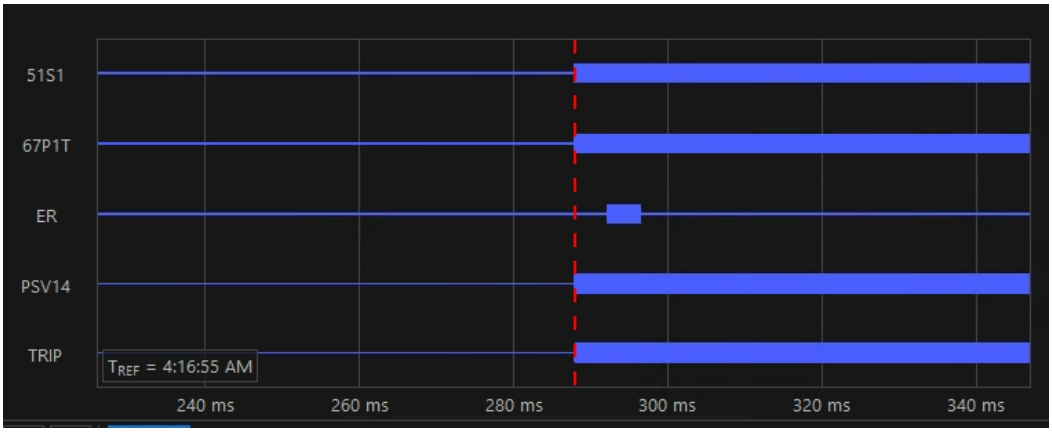

Figure 6. Relay function tripping signal under a circuit breaker internal fault

When a three-phase-to-ground fault occurred on the 34.5 kV bus, the fault current flowed from the PV inverter terminal to the fault location through the two CTs. The CT current RMS fault response under a three-phase-to-ground bus fault is shown in **Error! Reference source not found.**. It can be seen that the current RMS values on both CTs had only a small increase, due to the impact of the inverter current loop PI controller and its saturation limit. The fault current signals sent to the SEL-451 relay will always remain below the inverse-time overcurrent function threshold of 1.8 A, which means the overcurrent elements will not operate, and the relay hardware will not be able record the fault event on the bus. No trip signal will be generated under this scenario, the circuit breaker will stay closed during the fault, and the PV farm will continue to supply the power load.

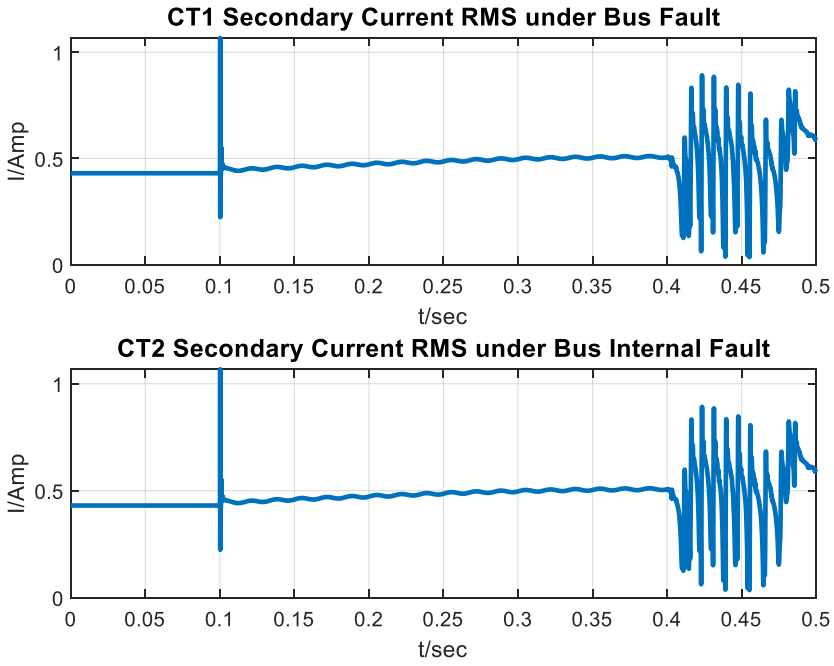

Figure 10. CT current RMS under bus fault

V. CONCLUSION

In this paper, a real-time hardware-in-the-loop simulation on the RTDS platform was performed with the programmable SEL-451 relay device. The purpose was to validate the relay scheme in a Dominion Energy virtual substation under a high level of PV penetration. Three-phase fault was applied at different locations of the substation system: inside the PV facility, inside the circuit breaker and on the 34.5 kV bus. The fault current simulated in RSCAD was transmitted to the doble to amplify the current signal and then sent to the SEL-451 relay, thus completing the open phase simulation. The operation of relay functions during the fault was recorded and evaluated. The relay scheme could detect a PV internal fault and generate an instantaneous tripping signal to isolate the faulted PV facility from rest of substation grid. During a circuit breaker internal fault, the circuit breaker fault detection element operated immediately, due to the current magnitude difference on the bus-side and line-side CTs. The fault current output from the PV inverter only had a small increase due to the impact of the control loop saturation, which was below the overcurrent threshold. Therefore, the SEL-451 wasn't able to detect and record the fault event.

For future work, it is recommended that HIL simulation of relay testing, using the same virtual substation, be conducted using the OPAL-RT simulator. The simulation results from RTDS will work as a benchmark to ensure the accuracy of the technician training model at the Dominion Energy Training Center.

BIBLIOGRAPHY

[1] M. S. Almas, R. Leelaruji and L. Vanfretti, "Over-Current Relay Model Implementation For Real Time Simulation & Hardware-In-The-Loop (HIL) Validation," IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society, 2012, pp. 4789-4796, doi: 10.1109/IECON.2012.6389585.

[2] A. S. Makhzani, M. Zarghami, B. Falahati and M. Vaziri, "Hardware-In-The-Loop Testing Of Protection Relays In Distribution Feeders With High Penetration of DGs," 2017 North American Power Symposium (NAPS), 2017, pp. 1-6, doi: 10.1109/NAPS.2017.8107191.

[3] C. S. Edrington, M. Steurer, J. Langston, T. El-Mezyani and K. Schoder, "Role of Power Hardware in the Loop in Modeling and Simulation for Experimentation in Power and Energy Systems," in Proceedings of the IEEE, vol. 103, no. 12, pp. 2401-2409, Dec. 2015, doi: 10.1109/JPROC.2015.2460676.

[4] G. Li, D. Zhang, Y. Xin, S. Jiang, W. Wang and J. Du, "Design of MMC Hardware-In-The-Loop Platform And Controller Test Scheme," in CPSS Transactions on Power Electronics and Applications, vol. 4, no. 2, pp. 143-151, June 2019, doi: 10.24295/CPSSTPEA.2019.00014.

[5] S. Palla, A. K. Srivastava and N. N. Schulz, "Hardware in the Loop Test for Relay Model Validation," 2007 IEEE Electric Ship Technologies Symposium, 2007, pp. 449-454, doi: 10.1109/ESTS.2007.372125.

[6] R. O. Salcedo, J. K. Nowocin, C. L. Smith, R. P. Rekha, E. G. Corbett, E. R. Limpaecher, and J. M. LaPenta, “Development Of A Real-Time Hardware-In-The-Loop Power Systems Simulation Platform To Evaluate Commercial Microgrid Controllers.” MIT Lincoln Laboratory Lexington United States, 2016.

[7] R. Stanev, K. Viglov, K. Nakov and T. Asenov, "A Real Time Power Hardware in the Loop Test Bed for Power System Stability Studies," 2020 12th Electrical Engineering Faculty Conference (BulEF), 2020, pp. 1-5, doi: 10.1109/BulEF51036.2020.9326020.

[8] S. R. Lee, E. Y. Ko, J. Lee and M. Dinh, "Development and HIL Testing of a Protection System for the Application of 154-kV SFCL in South Korea," in IEEE Transactions on Applied Superconductivity, vol. 29, no. 5, pp. 1-4, Aug. 2019, Art no. 5602104, doi: 10.1109/TASC.2019.2897838.

[9] G. Ravikumar, B. Hyder and M. Govindarasu, "Efficient Modeling of HIL Multi-Grid System for Scalability & Concurrency in CPS Security Testbed," 2019 North American Power Symposium (NAPS), 2019, pp. 1-6, doi: 10.1109/NAPS46351.2019.9000259.

[10] A. Avalos, A. Zamora, O. Escamilla and M. R. A. Paternina, "Real-time Hardware-in-the-Loop Implementation for Power Systems Protection," 2018 IEEE PES Transmission & Distribution Conference and Exhibition - Latin America (T&D-LA), 2018, pp. 1-5, doi: 10.1109/TDC-LA.2018.8511771.

[11] R. Liu, R. Sun and M. Tania, "Hardware-in-the-Loop Relay Testing in Dominion's Blackstart Plan," 2017 IEEE Power & Energy Society General Meeting, 2017, pp. 1-5, doi: 10.1109/PESGM.2017.8274184.

[12] "IEEE Standard for Inverse-Time Characteristics Equations for Overcurrent Relays," in IEEE Std C37.112-2018 (Revision of IEEE Std C37.112-1996) , vol., no., pp.1-25, 5 Feb. 2019, doi: 10.1109/IEEESTD.2019.8635630.

[13] Y. Jiao and F. C. Lee, "LCL Filter Design and Inductor Current Ripple Analysis for a Three-Level NPC Grid Interface Converter," in IEEE Transactions on Power Electronics, vol. 30, no. 9, pp. 4659-4668, Sept. 2015, d