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Enhanced Protection Modeling Approach for Power System Transient Stability Studies Using Individual Phase and Sequence Voltages

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SUMMARY

Accurate protection modelling in power system transient stability studies is required to ensure that reliable conclusions are drawn from such analyses. Typically, protection models available in transient stability programs use only positive sequence quantities such as the positive sequence voltages, currents, etc. to trigger any preventive/corrective actions such as tripping of generators, load-shedding, etc. However, with the increasing penetration of inverter-based resources, these models could prove to be inadequate in some scenarios. The work reported in this paper uses improved modelling practices for protection elements in transient stability studies using sequence/individual phase quantities. This approach does not necessarily require additional data from users and incurs only minimal incremental computational costs. In addition to using the sequence voltages/currents or individual phase voltages/currents for more accurate representation of protection systems, simply monitoring these quantities can also provide useful additional information about the system. Additionally, having access to these quantities could be useful in more accurate modelling of inverter-based resources such as the ability to model converter controls' protective functions, controls that actively suppress the negative sequence current produced by the inverter, and other such controls that use or control the negative sequence or zero sequence current injections.

In the absence of negative sequence and zero sequence network data, some typical assumptions based on engineering judgement are used to approximate this data. Once the data is available for all three sequence networks, the RMS sequence voltages (and currents) can be easily computed in the time-frame when an unbalanced fault is applied during a dynamic simulation. Since the network is assumed to be balanced before an unbalanced fault is applied and after it is cleared, the non-positive sequence voltages and currents in those time-frames are zero and all three phase voltages have equal magnitudes. Using this feature, two protection models widely used in dynamic simulation studies that are present in all commercial transient stability programs are modified in this work to use the lowest/highest individual phase voltage instead of positive sequence voltage to trigger trip signals. Even though the proposed models/techniques would have an impact in the relatively short time frame when an unbalanced fault is on in the system, it could have a significant impact on studies involving delayed clearing of faults. While it is not practical to model entire interconnection-wide base cases in a detailed three-phase domain for all transient stability studies, the proposed approach is aimed at trying to achieve a middle ground, such that more information about the system behaviour is obtained and protection systems are more realistically represented in RMS studies. These models are incorporated into a commercial positive sequence dynamic simulation engine GE-PSLF. Case studies using these models in two Western Electricity Coordinating Council (WECC) cases and a 9-bus case are discussed. With the framework to compute sequence/phase voltages/currents in place, the approach can be easily extended to models other than those mentioned in this paper. The possible future uses of such modelling capabilities for improved modelling of inverter controls etc. are also discussed.

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KEYWORDS

Protection modelling, Dynamics studies, Sequence voltages, unbalanced faults, phase voltage-based tripping.

INTRODUCTION

One of the recent topics of research focus in the power system industry has been understanding the behaviour of protection relaying elements or inverter protective functions in the grid under increasing penetration levels of inverter-based resources (IBRs), and ensuring reliable fault detection for such scenarios [1] - [7]. Inverter-based resources restrict their fault current contribution to be close to their rated current injection (typically less than 1.5 pu), which makes fault detection difficult [3], [5]. Additionally, some controls in modern converters are designed to inject very limited negative sequence currents under faulted conditions as compared to traditional machines [5]. Hence the fault detection techniques used in protection systems in emerging grids could also be different than traditional protection systems. For example, the negative sequence voltage generated by inverters to negate that seen at the terminals such that the negative sequence current injected by the inverter is zero, is proposed to be used to detect unbalanced faults in [4]. Zero-sequence based protection is proposed to be used in [5] to detect unbalanced faults in cases where the load unbalance is not very high, while the zero-sequence current magnitude on the high-side of the step-up transformer along with under-voltage detection is proposed to be used in [6]. An elaborate fault detection methodology using phase as well as sequence voltages has been proposed and tested on a hardware-in-the-loop setup in [1].

For typical dynamics studies, the network is assumed to be balanced before and after any unbalanced disturbances are cleared. Consequently, these studies typically involve the representation of positive-sequence networks and models only. Hence the state-of-the-art protection models in transient stability studies, such as those used for generator protection, load shedding, etc., also use only positive sequence voltages and currents to trigger tripping actions. However, since a vast majority of the faults seen on the system are unbalanced, monitoring/using only positive sequence quantities can be inadequate in some situations, especially for studies involving delayed clearing of the faults. The changing fault response of the system with several utility scale renewable energy resources as well as distributed energy resources using converter technologies, could render some of the traditional dynamic models inadequate in terms of sufficiently capturing controller actions that could have a noticeable effect on the post-fault system behaviour, which could in turn lead to misleading conclusions drawn from the results of such simulations. The voltages of the un-faulted phases in the vicinity of the fault may reach very high levels, likewise the faulted phase voltages may reach very low levels causing high phase currents. These severe conditions may persist for a duration sufficiently long to trigger tripping actions by the protection elements or protective functions in IBR controllers. Likewise, there may be some protection elements utilizing the negative sequence voltages/currents, and if standard positive sequence protection models are used for dynamic simulations, one could fail to predict the loss of some units.

In this work, the sequence voltages are computed using the positive-, negative- and zero-sequence networks during the timeframe that an unbalanced fault is on in the system. Since the network admittance matrices are built and factorized only when there is a network change, the additional computational expense of such capabilities is not significant. For the Western Electricity Coordinating Council (WECC) cases used in this work, the execution time needed on average is similar to that when only positive sequence quantities are computed. Next, the "*der_a*" model (described in detail in [9]) meant to represent distributed energy resources in bulk system studies is modified to use the lowest/highest phase voltage in the voltage cut-out logic that is meant to capture momentary cessation. Similarly, one of the most widely used generator protection models in dynamics studies, "*lhvrt*" that is meant to model the protection for generators against low/high voltages, is modified. In the modified version of the model trip signals are triggered based on the lowest/highest individual phase voltage instead of the positive sequence voltage. A meter model is also implemented as a part of this work, to monitor the sequence voltages or individual phase voltages at the buses/areas/zones of interest. Case studies are presented using WECC cases to demonstrate the advantages of such modelling. Other applications of such modelling techniques such as more detailed converter models are also discussed.

SEQUENCE NETWORK ASSUMPTIONS

One of the challenges in obtaining all sequence/phase quantities is that often the zero-sequence and negative-sequence network data are not mapped to the positive sequence network data used in dynamic simulations. Since the zero sequence and negative sequence representations of the system are necessary for the computation of these sequence/per-phase voltages and currents, if this data is not readily available some standard engineering assumptions are employed to approximate the negative sequence and zero sequence network data using the available positive-sequence data. These are standard assumptions made in typical short circuit analysis studies and are listed in this section. The negative sequence impedances for generators are assumed to be equal to their respective positive sequence impedances. Generators are assumed to be open-circuited for zero sequence networks as most generator step-up (GSU) transformers are connected in delta on the generator side. All transformer connections are assumed to be wye-grounded except on the generator-side for GSUs which are assumed to be in delta. The negative sequence and zero sequence transformer impedances are assumed to be equal to the positive sequence impedances. For transmission lines, the negative sequence impedances are assumed to be equal to the positive sequence impedances and the zero-sequence impedances are assumed to be thrice the positive sequence impedances. The zero-sequence charging shunt admittances for transmission lines are assumed to be half that of the positive sequence charging shunt admittances while the negative sequence charging shunt admittances are assumed to be equal to the positive sequence charging shunt admittances. Loads and shunts are assumed to be constant admittance in the negative sequence network with the same admittance as they would have in positive sequence, while they are assumed to be open circuited in the zero-sequence network. In the duration that an unbalanced fault is applied, the source of unbalance is assumed to be only at the faulted location (i.e. loads and the rest of the network are still assumed to be balanced). The sequence network interconnections for single-line-ground (SLG) faults, line-line (LL) faults, and line-line-ground (LLG) faults are standard, as available in several references and shown in Figure 1 [8]. With the positive, negative, and zero sequence current injections at the faulted location known, the sequence voltages and currents throughout the network can easily be computed. The sequence voltages/currents can then be used to obtain the phase A, B, C voltages/currents using the standard transformation matrix [10]. For a 9-bus simplified representation of the western interconnection [11], the phase A, B, C, and positive sequence voltages for an SLG bus fault at bus 6 are shown in Figure 2. The negative sequence voltage seen at the terminals of a photovoltaic (PV) plant in a full WECC case for an SLG fault is shown in Figure 3.

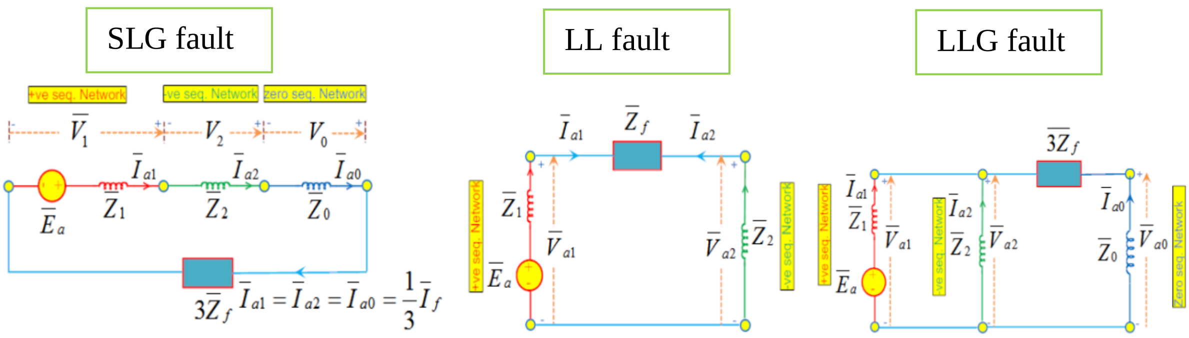

Figure 1 Network interconnections for unbalanced faults [8]

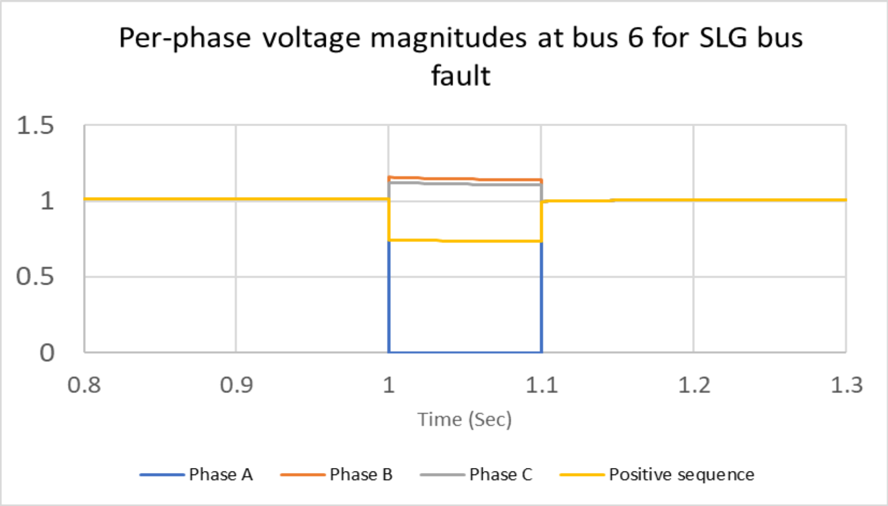

Figure 2 Individual phase voltages for a single-line-ground fault at bus 6

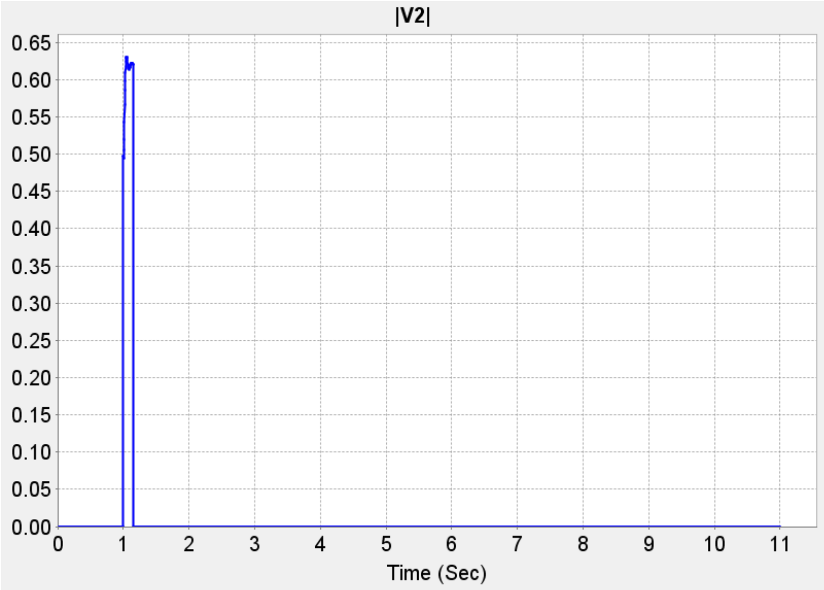

Figure 3 Negative sequence voltage (pu) seen at the terminal of the PV units in WECC case

CASE STUDIES

In this section, some examples will be shown to demonstrate the modified models. The *der_a* is the latest WECC-approved model to represent an aggregation of DERs including utility-scale DER (U-DER) as well as retail-scale DERs (R-DER) along a feeder [9]. The model has also been recently included as a component in the composite load model (*cmpldw*). One of the salient features of this model is its capability to capture momentary cessation and tripping of these resources on high/low voltages. This voltage cut-out block uses the positive-sequence voltage to send either trip signals or reduced current signals as shown in Figure 4. The output of this block *vmult* is multiplied with the current command signal to obtain the actual current injection into the network. The signal *vmult* tracks the black line defined by the points (*vl0*,0), (*vl1*,1),(*vh1*,1), and (*vh0*,0) unless the following conditions occur:

- If the voltage stays below *vl1* for a duration greater than *tvl1*, *vmult* will follow the path of the red line when the voltage recovers. *Vmin* is the lowest voltage (greater than *vl0*) during a simulation after timer *tvl1* expires.

- If the voltage stays above *vh1* for a duration greater than *tvh1*, *vmult* will follow the path of the red line when the voltage recovers. *Vmax* is the highest voltage (lesser than *vh0*) during a simulation after timer *tvh1* expires.
- If the voltage *Vt_flt* stays below *vl0* for more than *tvl0* seconds or if it stays above *vh0* for more than *tvh0* seconds, then *vmult* will remain at zero i.e. the DERs are completely trippped.

The frequency trip action of the model is fairly straightforward where if the frequency seen at the terminals of the DER falls below the parameter *fltrp* for more than *tfl* seconds or increases more than *fhtrp* for more than *tfh* seconds, the DERs are entirely tripped.

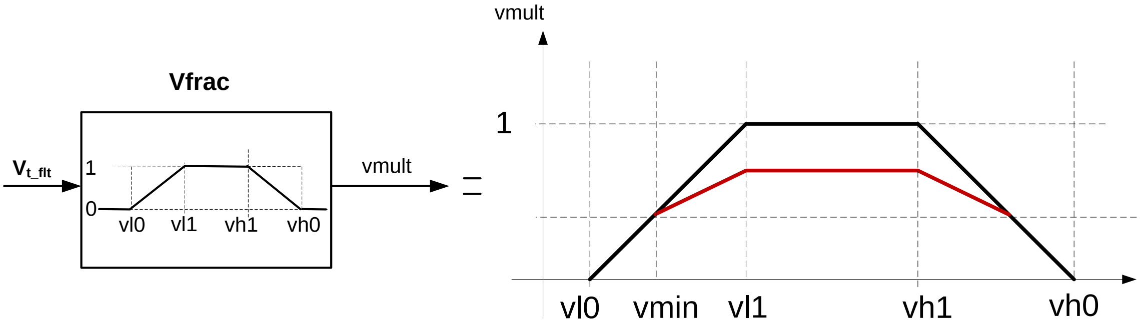

Figure 4 Voltage cut-out function in *der_a* model

However, it is important to note that this model could be used to represent an aggregation of DERs on all three phases and not all phases see the same voltage for unbalanced faults. Hence in the proposed "*der_a_ph*" model, all other aspects are the same as the *der_a* model, except that the model uses the highest of the three phase voltages for high-voltage protection and lowest of the three phase voltages for low-voltage protection. The parameters used for the *der_a* model are obtained from the NERC guideline [9], and the parameters pertinent to the momentary cessation/trip settings are provided in Table 1. Note that in the *der_a_ph* model used in this section while the entire unit is tripped on over/under-voltage, since only the DERs on the phases with extreme voltages are tripped it would be more realistic to trip only a fraction of the net DER output for individual phase violations.

This modified model was used in a small 9-bus system with three generators, one of which was modelled using *der_a_ph*. A 10-cycle solid SLG fault was applied one bus away from the DER terminals i.e. on the high-side of its step-up transformer. The phase A, B, C and positive sequence voltages are shown in Figure 5. Phase A being assumed to be the faulted phase for SLG faults in PSLF, phase A voltage is much lower than the other two phases as seen in Figure 5, while the other two phase voltage magnitudes are higher than the positive sequence voltage which is shown in blue. As expected, before the unbalanced fault is applied and after it is cleared, all three phase voltage magnitudes match the positive sequence voltage magnitude. It is seen that the lowest phase voltage drops below *vl1* for more than *tvl1* seconds and hence the output of the DER is reduced from 160 MW to about 60 MW when the fault is applied and remains at that value for about 4 s, as shown in Figure 6. This reduced output causes the frequency to gradually decline, until the *fltrp* threshold is crossed at about 2.79s, causing the DER to completely trip on under-frequency at about 4.79s once the timer *tfl* times out. The output of the voltage cut-out block, output of the frequency trip block, as well as the frequency seen at the DER terminal are shown in Figure 7. In the case of *der_a* model however, since the positive sequence voltage never decreases below *vl1*, its output recovers as soon as the fault is cleared and hence the frequency remains above the trip threshold throughout the simulation causing the unit to remain online throughout the simulation.

Table 1 Trip/cut-out parameters used for *der_a*/*der_a_ph* models

Parameter name	Description	Value
vl0	Voltage break-point for low voltage cut-out of the inverter	0.44 p.u.
vl1	Voltage break-point for low voltage cut-out of the inverter	0.49 p.u.
vh0	Voltage break-point for high	1.20 p.u.

	voltage cut-out of the inverter	
vh1	Voltage break-point for high voltage cut-out of the inverter	1.15 p.u.
tvl0	Low voltage cut-out timer	0.16 s
tvl1	Low voltage cut-out timer	0.16 s
tvh0	High voltage cut-out timer	0.16 s
tvh1	High voltage cut-out timer	0.16 s
vrfrac	Fraction of device that recovers after voltage returns within vl1 and vh1	0
fltrp	Low frequency threshold for cut-out of the inverter	59.3 Hz
fhtrp	High frequency threshold for cut-out of the inverter	60.5 Hz
tfl	Low frequency cut-out of timer	2.0 s
tfh	High frequency cut-out of timer	2.0 s

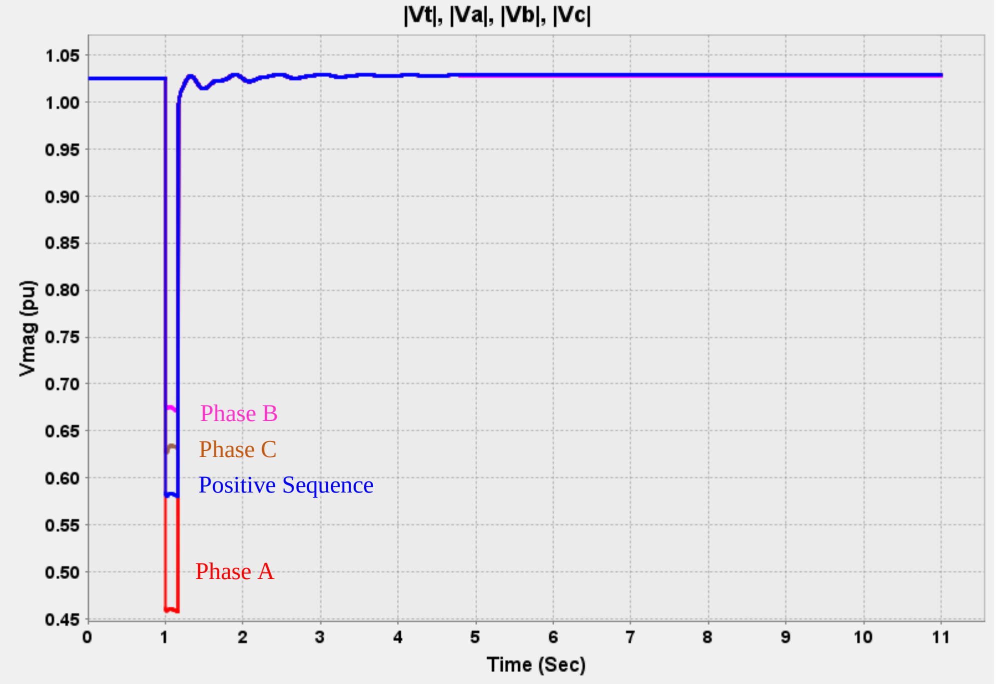

Figure 5 Phase A, B, C and positive sequence voltages at the DER terminal

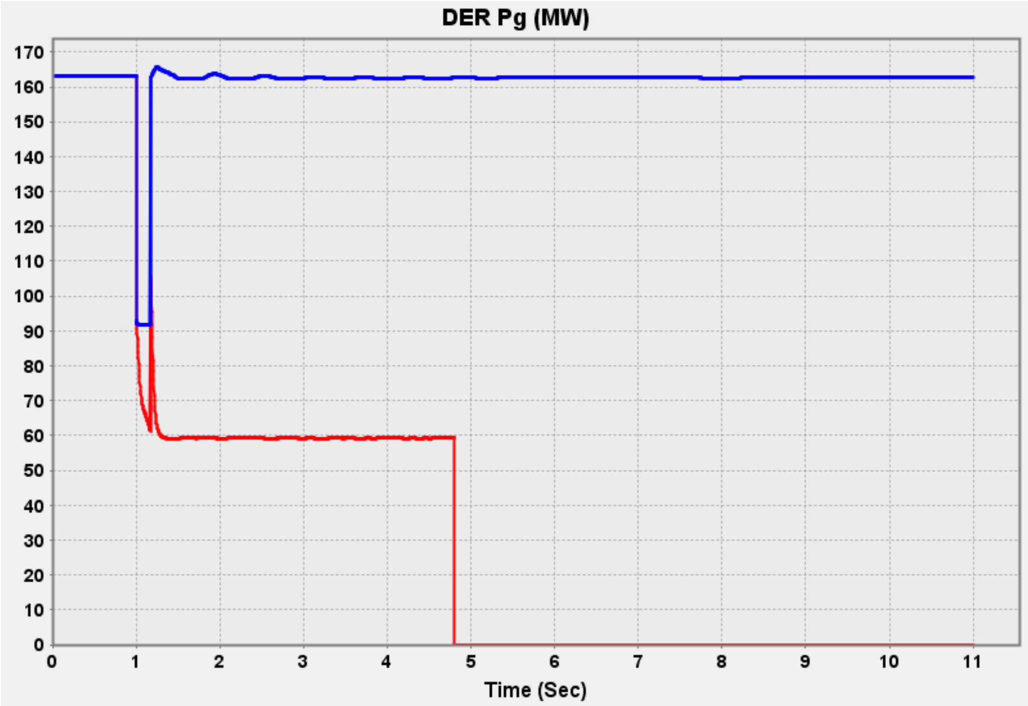

Figure 6 DER output : Blue : *der_a* model, Red : *der_a_ph* model.

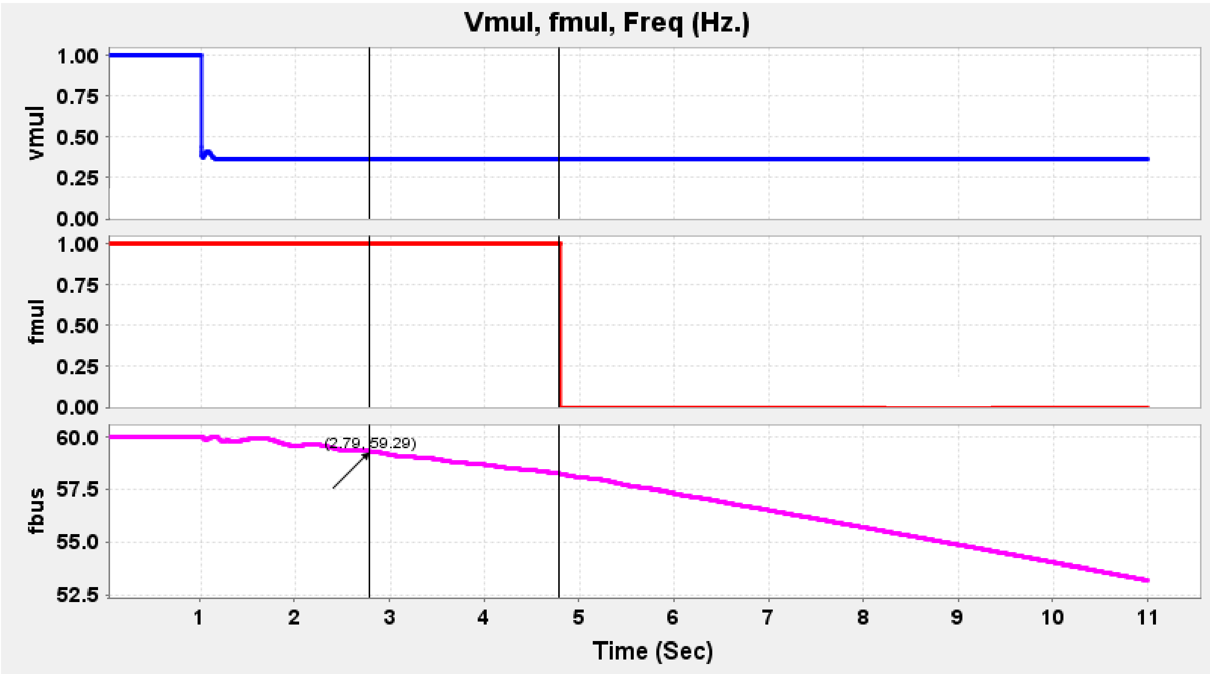

Figure 7 DER output : Blue : *vmul* (output of voltage cut-out block), Red : *fmul* (output of the frequency trip block), Pink : Frequency at the DER terminal bus in Hz.

It is seen that the lowest phase voltage is very close to *vl0*, hence if the voltage cut-out settings were to be slightly tighter, the DER would have entirely tripped on under-voltage by the time the fault cleared. This is shown in Figure 8 where the *vl0* and *vl1* values are 0.47 pu and 0.52 pu respectively. It can be seen that the lowest phase voltage drops below *vl0* for more than *tvl0* seconds, causing the DER to trip entirely when the *der_a_ph* model is used, whereas the *der_a* model output recovers once the fault is cleared.

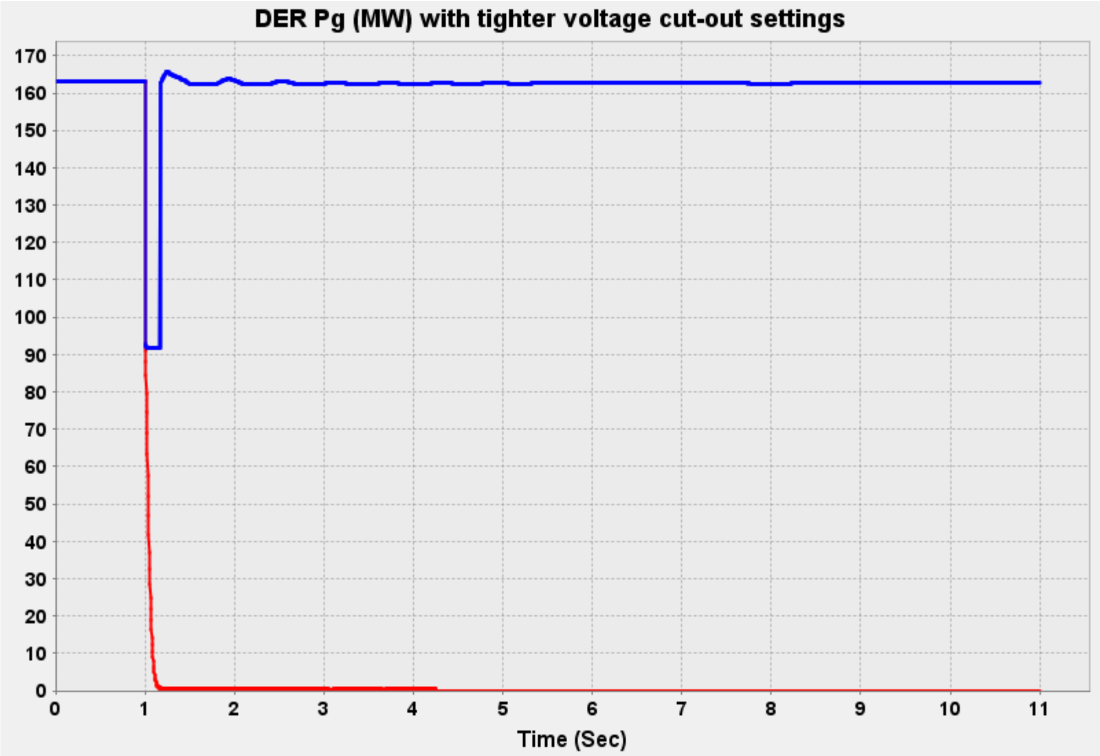

Figure 8 DER output with *vl0*=0.47, *vl1*=0.52 : Blue : *der_a* model, Red : *der_a_ph* model.

Similarly, the relay model typically used for representing high/low voltage protection for utility-scale power plants (thermal as well as renewable plants), *lhvrt*, is modified to use the highest/lowest phase voltages instead of the positive-sequence voltage to determine trip signals. The model *lhvrt* has the provision of including up to ten voltage trip settings, each with its own fixed-timer setting. The modified model was used in a WECC case for all instances of *lhvrt* and a 9-cycle single-line-ground fault was applied at the high-side bus of the step-up transformer for two PV plants. The *lhvrt* models for the protection of these two units had eight trip settings, and the relevant one in this study was a delta voltage threshold of -0.55 pu with a timer of 0.15 s i.e. if the voltage decreases below 0.45 pu for more than 0.15 s, the unit is to be tripped in the simulation. The *dV* signals monitored by the two versions of the model (using positive sequence voltage vs. lowest phase voltage) are shown in Figure 9. It is seen that while the positive sequence reaches a nadir of approximately 0.55 pu, the lowest phase voltage reaches a nadir of approximately 0.1 pu. Both units trip on under-voltage based on the lowest phase voltage when the modified model is used, whereas neither trip when the original model is used. The real power output of one of the units is shown in Figure 10, where the blue curve is obtained using the original *lhvrt* model, while the red curve is obtained using the modified version.

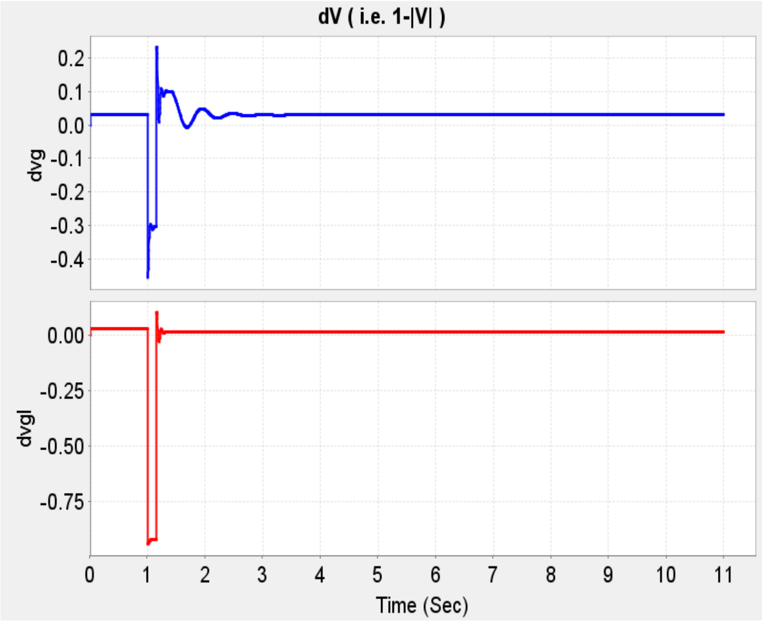

Figure 9 Voltage deviations (1-|*V*|) pu seen by *lhvrt* : Blue : Positive sequence voltage deviation, Red : Lowest phase voltage deviation.

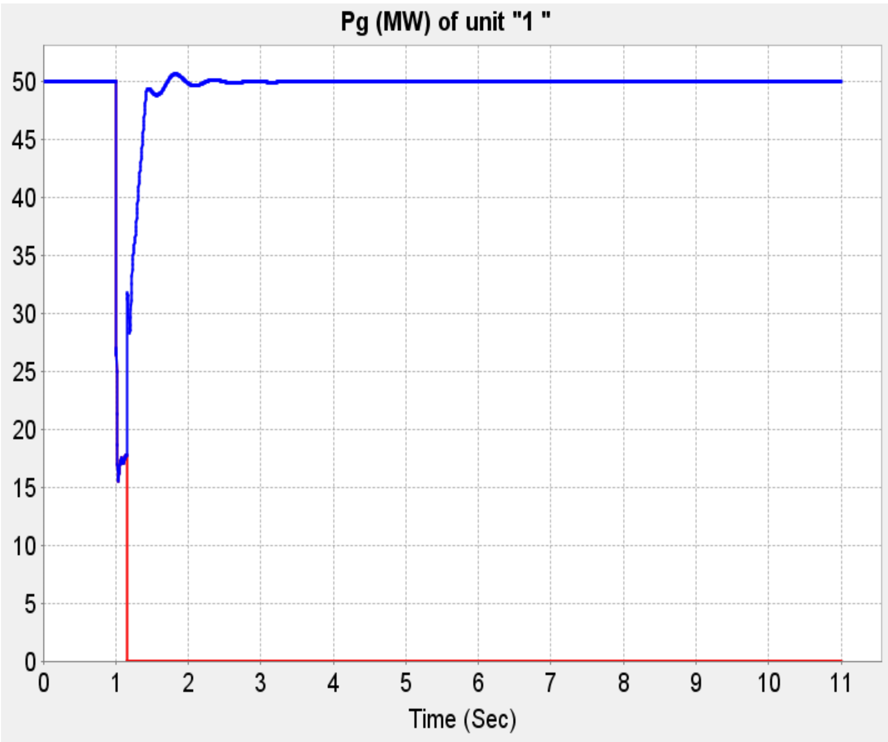

Figure 10 Output of one of the PV units: Blue : Original *lhvrt* model, Red : Modified *lhvrt* model using phase voltages.

For a different WECC case, a 10-cycle solid LLG fault is applied at the terminals of a PV plant generating 155MW. There are four trip settings of the *lhvrt* model for this unit: delta voltage thresholds of -0.5 pu and 0.2 pu, both with a timer of 0.16s, -0.12 pu with timer of 2s, 0.1 pu with timer of 1s. The positive sequence voltage and phase voltage magnitudes at the terminal of the plant are shown in Figure 11. It is seen that while the positive sequence always remains between 0.5 pu and 1.0 pu, the faulted phase voltages (phases B and C) reach 0 pu, while the highest phase voltage magnitude for phase A is larger than 1.5 pu. Since both the trip criterion of delta voltage less than -0.5

pu and greater than 0.2 pu are satisfied, the unit trips when the modified model is used, while it does not with the original model, as seen from Figure 12.

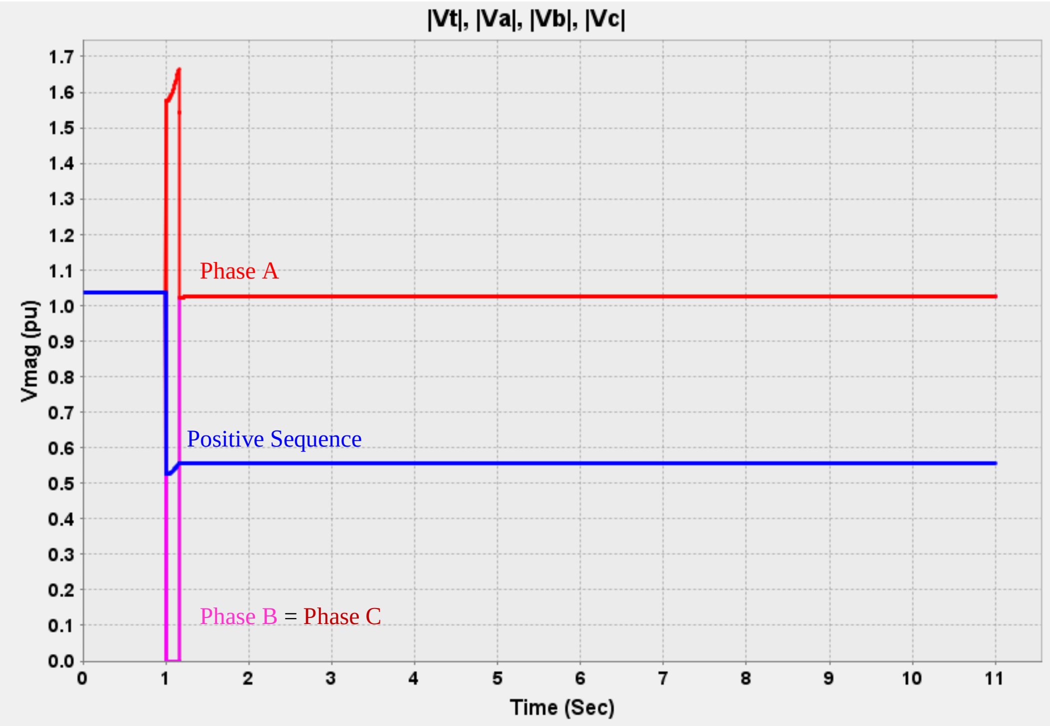

Figure 11 Phase A, B, C and positive sequence voltages at the PV terminal for LLG fault

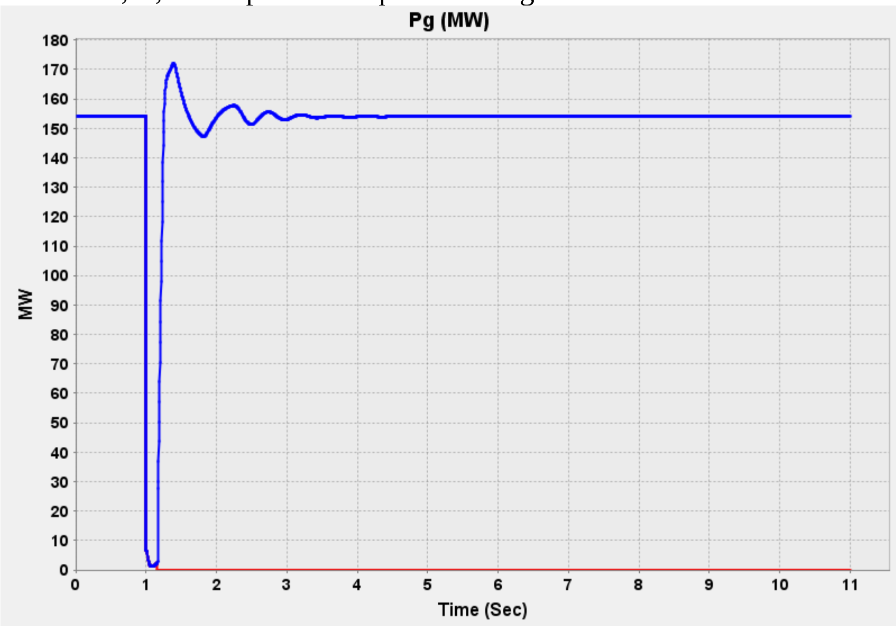

Figure 12 Output of the PV unit for LLG fault: Blue : Original *lhvrt* model, Red : Modified *lhvrt* model using phase voltages.

OTHER APPLICATIONS OF SUCH "PHASE QUANTITY-BASED"/ "SEQUENCE QUANTITY-BASED" MODELS

Even monitoring the phase and sequence quantities without triggering any protection models using these quantities can provide very useful information while analysing the results of dynamic simulations. A major challenge with the modelling of distributed energy resources in positive sequence models is to appropriately parameterize the trip settings in the models such as the *der_a* model, to capture the spread of DERs along a feeder each seeing a different terminal voltage and to capture the effects of unbalanced faults appropriately. The proposed models using phase voltages for modelling the voltage cut-out block representing momentary cessation in *der_a_ph* can make considering unbalanced faults easier during parameterization. The negative sequence quantity- and zero sequence quantity-based protection can also be modelled more accurately with such modelling approaches. Using the additional signals described, negative sequence current relay operation in conventional generators could be estimated during prolonged unbalanced conditions, such as a single line reclosing. The signals could also be used to capture motor contactor opening/closing actions more accurately. Additionally, these approaches can be easily extended to models other than those mentioned in this paper. For instance, most inverters have active controls to zero out the negative sequence voltage at the terminals, such that the negative sequence current at the inverter terminals is zero [5], [7], which may be modelled using such a capability. Additionally, as more and more loads in the grid become drive-connected, one could also possibly take advantage the sequence/phase quantities to capture the behaviour such variable frequency drives more accurately in their models.

CONCLUSIONS

The work presented in this paper explores a more realistic representation of protection elements in dynamics studies, using phase voltage magnitudes and not just positive sequence voltage magnitudes. While the quantities are still in the RMS domain, they give a clearer picture of the system behaviour than using only positive sequence quantities. The sequence and per-phase voltage/current quantities can be obtained for unbalanced faults using available negative and zero sequence data or some standard assumptions to set up the sequence data. The additional computations involved for obtaining these per-phase/sequence voltages are minimal and do not add much to the execution times. Case studies are shown using modified versions of the *der_a* model modifying the momentary cessation portion of the model to use the lowest/highest voltage magnitude instead of the positive sequence voltage magnitude. Likewise, the *lhvrt* model was modified to use the lowest/highest phase voltage magnitude for determining trip signals instead of positive sequence voltage. It is shown using WECC cases that unbalanced faults can cause sufficiently high/low voltages in individual phases to cause trips which may not necessarily be seen in the positive sequence voltage based models. Thus, using such models one can get a more accurate grid response from the simulation. The use of sequence/phase voltage /current quantities can be easily extended to other models such as capturing advanced controls of inverters.

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