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Investigation and Correction of Phase Shift Delays in Power Hardware in Loop Real-Time Digital Simulation Testing of Power Electronic Converters

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SUMMARY

Power Hardware in Loop (PHIL) digital simulation testing has been recently introduced as an alternative approach to traditional methods of high power / high voltage device level testing without the use of load banks and physical medium/high voltage test feeders. PHIL testing approach is very cost effective and highly applicable for performance evaluation of power electronic apparatus in distribution and transmission systems such as power converters in PV and wind generation plants, energy storage systems, and distributed/transmission level power conditioning units and FACTS devices.

In PHIL testing, power hardware equipment selected for test, hereinafter called device-under-test (DUT), is virtually exchanging power with a power system at the point of interface represented in a real-time digital simulation environment. The main purpose of PHIL simulation is mimicking accurate operating characteristics of the associated power system (a distribution circuit or substation) during the performance evaluation tests, rather than representing the system with lump-sum equivalent impedances and voltage sources. Because of interacting with DUT through high power amplifiers, PHIL may encounter instability, poor performance, or low accuracy owing to phase shift or non-linearity of signal amplification schemes employed in typical power amplifiers.

In this paper, the most impacting issue of phase shift in a PHIL simulation setup is investigated. Then, a simple and effective compensation method is proposed for PHIL to overcome instability, poor performance, and inaccuracy induced by phase shift. PHIL simulation and experimental results have been provided for both steady-state test cases and transient phenomena to demonstrate the effectiveness and functionality of the suggested PHIL.

KEYWORDS

Power Hardware-in-loop (PHIL), Device-under-test (DUT), Phase Shift, Grid Simulator, Real-time Digital Simulation, Performance Evaluation, PV Inverters

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INTRODUCTION

To effectively study a power electronic device or a generation facility utilizing multiple power convertors, information about the control and protection capabilities of the device should be available [1]. The information should provide detail insights into expected dynamic response and the possible interactions with other devices to allow accurately performed power system impact studies. Such studies should include detailed faults analysis and voltage disturbance analyses. Knowledge of detailed device models and being able to characterize dynamic behavior of power electronic interfaces are expected to become more and more critical and raise many questions as new smart control functionalities and combining generation and power conditioning capabilities are introduced through emerging Smart Inverter technologies [2]-[5].

Power hardware-in-loop (PHIL) testing uses real-time digital simulation platforms and provides the ability to interface off-the-shelf commercial inverters and power electronic devices for closed loop performance testing. PHIL testing approach enables creation of realistic test conditions, which from the inverter point of view, are indistinguishable from those in the real-world environment. Hence, an accurate observation of inverter control responses and a full assessment of impact on the system will become possible [6]-[13].

There are still some challenges related to stability, performance, and phase shift of different signals in PHIL simulation, which could adversely impact the test results and deteriorate the expected outcome [2]-[3]. Finding and adding equivalent resistance and current in modelling, adding inductor in series with DUT, employing current filter, putting more burden on computation hardware, and applying PI controller were proposed before as described in [2]-[3]. However, mentioned methods are suffering from using exact time domain signal and simple approach with small computation burden and adding no additional controller, dynamics, and hardware for industrial applications of PHIL simulation.

In this paper, an investigation has been conducted on utilization of commercially available high power grid simulators as the power amplifier interface for closed loop testing of power hardware with real-time digital simulators. It will be shown that, even though a linear grid simulator was successfully selected and utilized for the tests, there is yet possibility of phase angle shift between generated voltage in the output of the grid simulator and the originally injected voltage signal from the real-time simulator. Any delay and phase shift in the closed loop test circuit can become a source of large power mismatch and resonance. Hence, a compensation method is suggested to achieve good stability and proper level of accuracy between real-time simulation and experimental tests. Through applying several steady-state and transient test cases, such as a short circuit fault, capacitor switching and load rejection, it has been shown that the suggested compensation method is effectively canceling the phase shift in all operating conditions without affecting the system response.

POWER HARDWARE IN LOOP TESTING APPROACH

Block diagram of a typical PHIL setup for PV inverter testing, as a commonly used example for this testing method, is shown in Figure 1. In this figure, the device under test (DUT) is an off-the-shelf, commercial three phase PV inverter (grid-tied) developed for the North American market and presently being installed on various distribution circuits. For the purpose of system impact evaluation and performance testing, the interconnecting 12 kV distribution circuit under study is modeled in a digital simulation environment. The PV inverter comes with an internally conditioned 480 VAC output. The 480 V three-phase connections to the real-time digital simulator for the inverter interface are provided through a grid simulator, carefully sized according to the kVA rating of the inverter under test.

In this application, the grid simulator acts as a regenerative, linear power amplifier, receiving low level voltage signals (±10V) from the real-time simulator and amplifying the signals to the inverter AC voltage range (480V in this case). Using this approach, the grid simulator will be able to sink current from the DUT (inverter) and re-circulate the PV power production back into the main power supply. This re-generative testing approach drastically reduces power consumption requirements and any need for extensive heat dissipation [1]-[15].

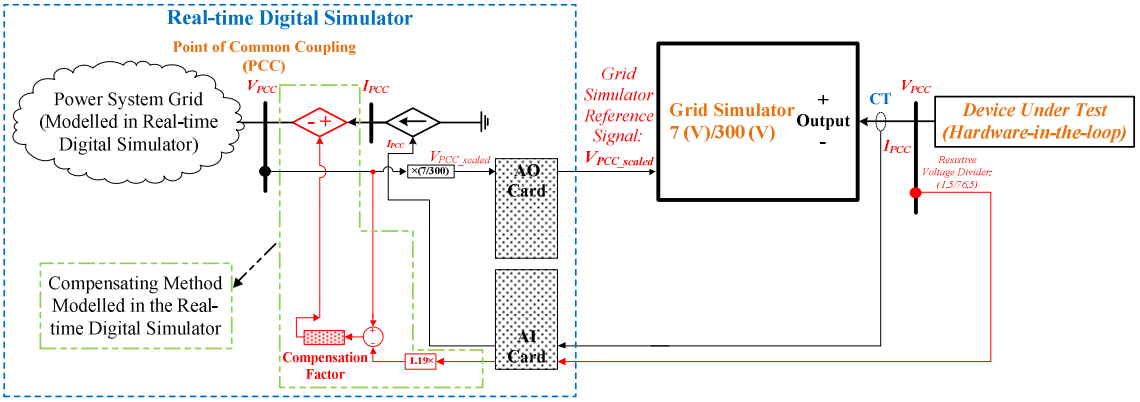


Fig. 1: Block diagram of a typical PHIL testing [1]-[15]

Any phase shift or signal distortion in the closed-loop control including the signal amplification and feedback current processing can introduce major errors in the test results or create unexpected and disruptive resonance.

This paper evaluate s any source of phase shift and distortion, whether it is introduced in the real time simulator platform, and/or issues through the power amplifier and voltage/current measurement instruments.

The grid simulator is a controllable variable voltage source that amplifies the analog signal from real-time digital simulator analog output (AO) card for driving power hardware in a real-time digital simulator closed loop. Although, the process of signal scaling and power amplification has been properly designed to ensure linearity, it was noted that there will be always a relatively large phase shift between injected signal and the amplified output signal. The presence of phase shift was verified by comparing the input signal to the amplifier from the AO card of real-time digital simulator and the signal received by the analog output (AI) card as the feedback measurement. Therefore, a compensation method has been suggested to overcome the mentioned problem to achieve accuracy and performance in PHIL testing approach.

PHASE SHIFT INVESTIGATION GENERATED BY DEVICE IN PHIL SIMULATION

In the first test, the AO card has been evaluated for delay in producing the output signal. To do so, a signal is produced and sent out by the AO card and it is read as feedback by the input channel of the AI card as shown in Fig. 2. Fig. 2 demonstrates the configuration of the implemented circuit.

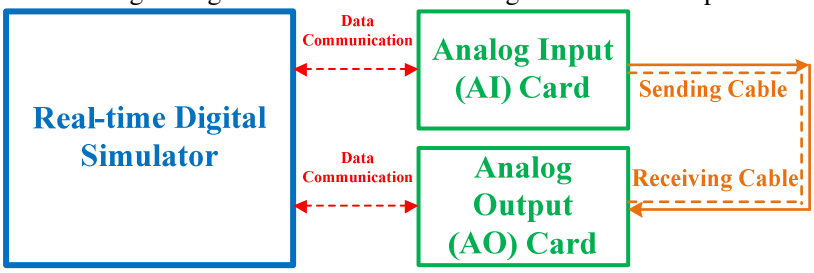


Fig. 2: Circuit configuration for testing generated delay by AI/AO cards in the typical real-time simulation.

In the above experiment, one 60 Hz sinusoidal signal was sent via the AO card, and that signal was immediately read by the AI card. Fig. 3 shows the two signals overlaid on the same graph. The phase shift between the two signals (output versus input) was measured. Multiple snap shots are presented in Fig. 3 to show the delay between AI signal and AO signal from the first test.

Voltage Sent out by AO Card; Voltage Received by AI Card

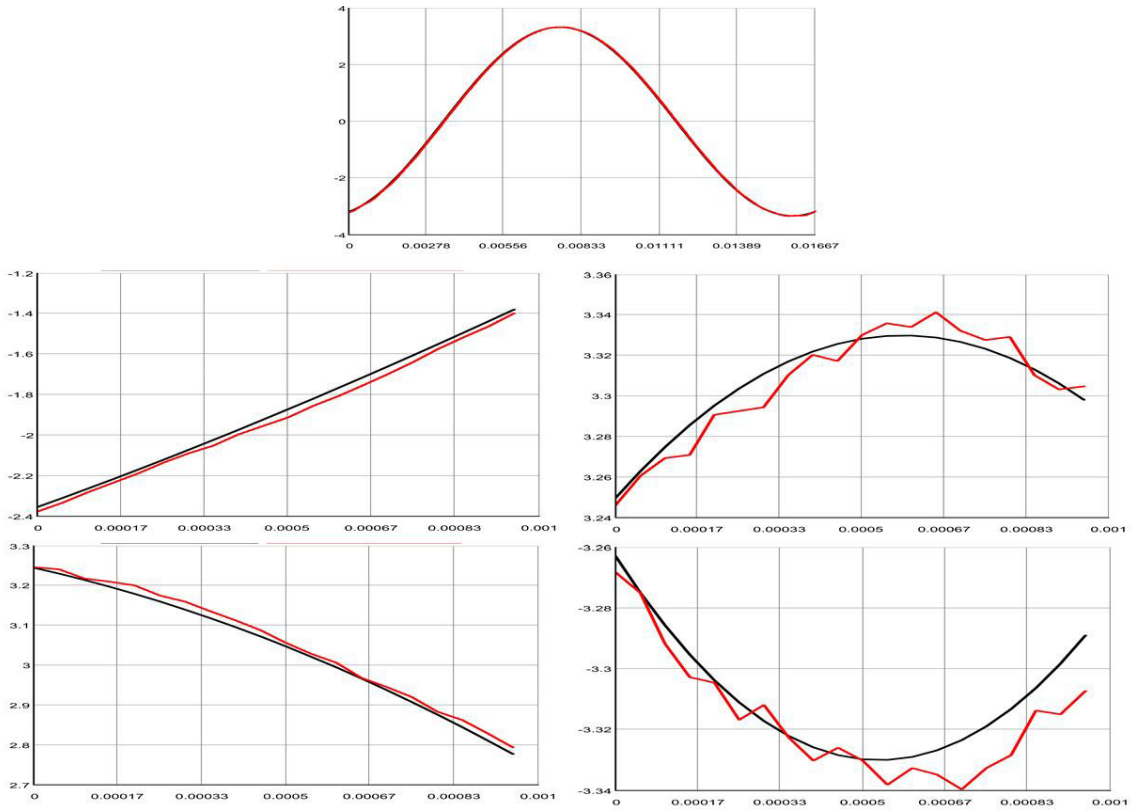


Fig. 3: Test results of delay generated by AI/AO cards; Black: Voltage Sent out by AO Card, Red: Voltage Received by AI Card

This test showed how much delay may be produced by real-time digital simulator cards. As it is clearly seen, the delay is around 35 µSec which amounts to 0.76˚ for a 60 Hz input signal. It should be noted that the simulation time step for the real time simulator in modeling typical power system cases is 50 µSec. Hence, this amount of phase shift is considered acceptable in representation of most power system phenomena.

In the second test, the AO signal was used to generate a 60 Hz sinusoidal reference signal for driving the grid simulator. Using the analog voltage input of the grid simulator, the signal is amplified by 300/7 gain, i.e. a scale factor of 42.857, to generate the output voltage up to 300 V rms (phase to neutral) from the reference signal with the voltage up to 7 V. Output voltage of grid simulator was passed through a resistive voltage divider with a gain of 0.019608 to scale it within the +/-10 V range, while preventing any delay regarding the measurement process. The scaled output signal from the voltage divider was finally read by AI card to insert into the real-time digital simulator. Once received in the simulation environment, inside the real-time digital simulator model, the signal is scaled back by a factor of 1.19 to the magnitude of the reference signal to be comparable as it is revealed in Fig. 4.

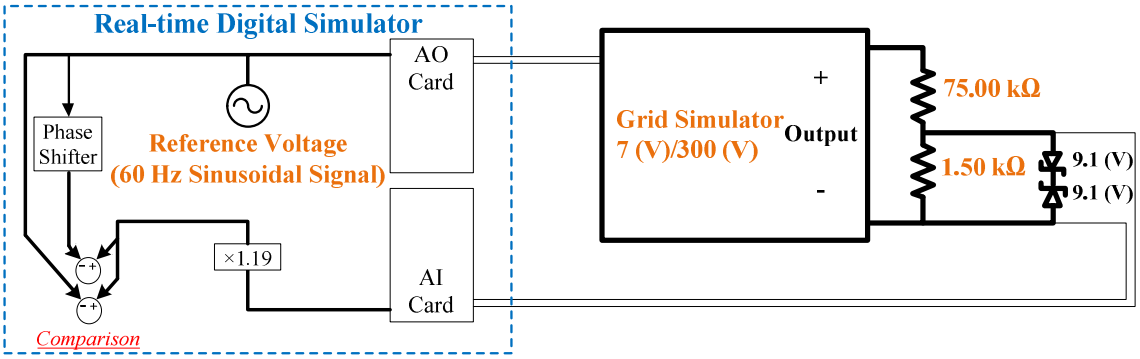


Fig. 4: Circuit configuration for testing generated delay by grid simulator in the typical real-time simulation and PHIL test.

Plotting measured voltage of the grid simulator's output after scaling back to the real-time digital simulator model and the reference signal sent by AO card showed that the phase shift between two signals was about 3.456˚ for the 60 Hz sinusoidal input signal. Consequently, the majority of phase shift is produced by the grid simulator; simple math shows that 2.706˚ phase shift is generated by the grid simulator, and the rest is generated by all cards, i.e. AI and AO. Measured voltage of the grid simulator's output voltage after scaling back in real-time digital simulator, the reference signal sent by AO, and phase shifted reference signal by 3.456˚ are depicted in Fig. 5. Moreover, the signal difference (error) between grid simulator's output voltage and reference signal is captured in Fig. 6 for 0˚ phase shifted signal and 3.456˚ phase shifted signal.

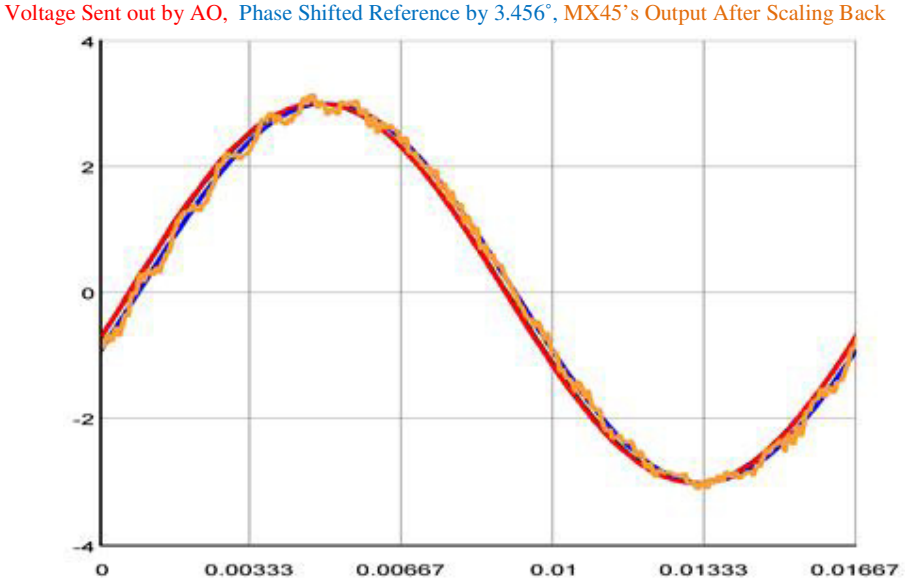


Fig. 5: Test results of delay generated by grid simulator; Red: reference voltage sent out by real-time digital simulator, Blue: reference voltage shifted by 3.456˚ and sent out by real-time digital simulator, Orange: voltage generated by grid simulator.

Error Signal before Shifting Phase, Error Signal after Shifting Phase by 3.456˚

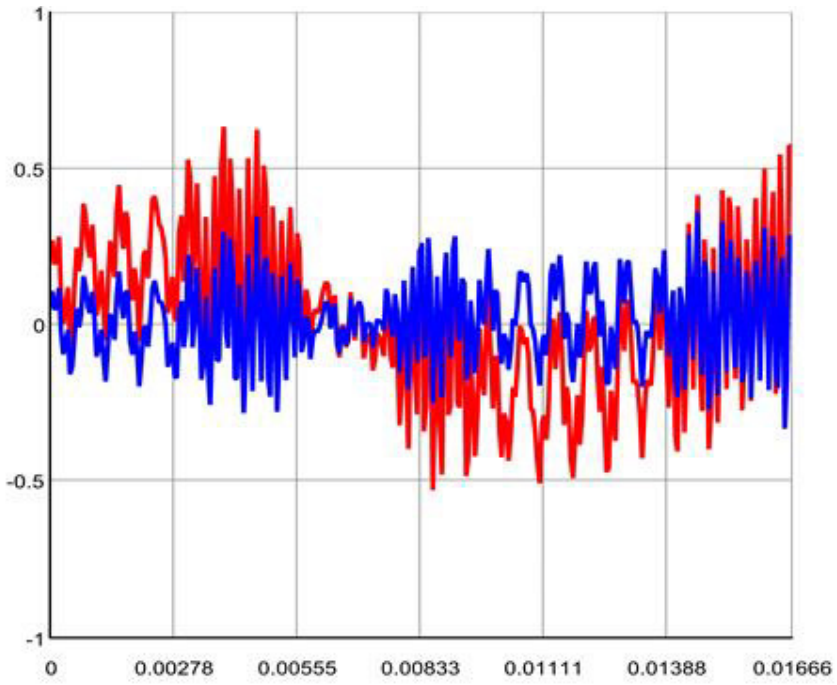


Fig. 6: Test results of error signal after shifting phase; Red: error signal generated by subtracting reference voltage sent out by real-time digital simulator and scaled back grid simulator voltage, Blue: error signal generated by subtracting 3.456˚ shifted reference voltage sent out by real-time digital simulator and scaled back grid simulator voltage.

PHASE SHIFT COMPENSATION GENERATED BY DEVICE IN PHIL SIMULATION:

The usual PHIL simulation was shown in Fig. 1 without considering the phase shift may be induced by either communication cards as well as device.

As shown in previous sections, there is phase shift between the generated voltage and sending reference signal by AO card. Consequently, the currents absorbed/injected by/into the device under test do not have the same phase angle with respect to the V_{PCC} in the model implemented in real-time digital simulator.

In order to compensate that issue, a compensation method is proposed by employing an additional voltage feedback in the PHIL real-time simulation. The proposed voltage feedback is made by reading the output voltage generated at the terminal of the device under test. Then, the generated voltage is scaled back to the device's reference signal applied in the real-time digital simulator model. Because of phase shift issue, there will be error between the two signals. That error has been employed in the PHIL real-time simulation to cancel the effect of device's phase shift and to achieve the original signal. Because the simulation is conducting in the real-time environment, it will be required to delay the error with one simulation time step. In other words, the error signal at time (t) is replaced with its value at time $t+T_s$ where T_s is the clock sampling time in real-time domain environment. The entire proposed method is demonstrated in Fig. 7.

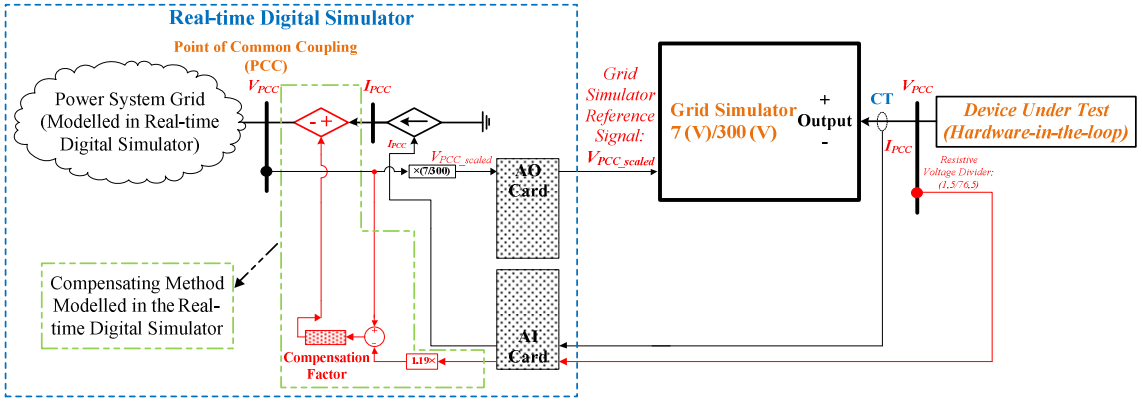


Fig. 7: The proposed PHIL simulation enhanced with voltage feedback

The voltage measurements for one phase of the circuit after applying the proposed compensating method are shown in Fig. 8.

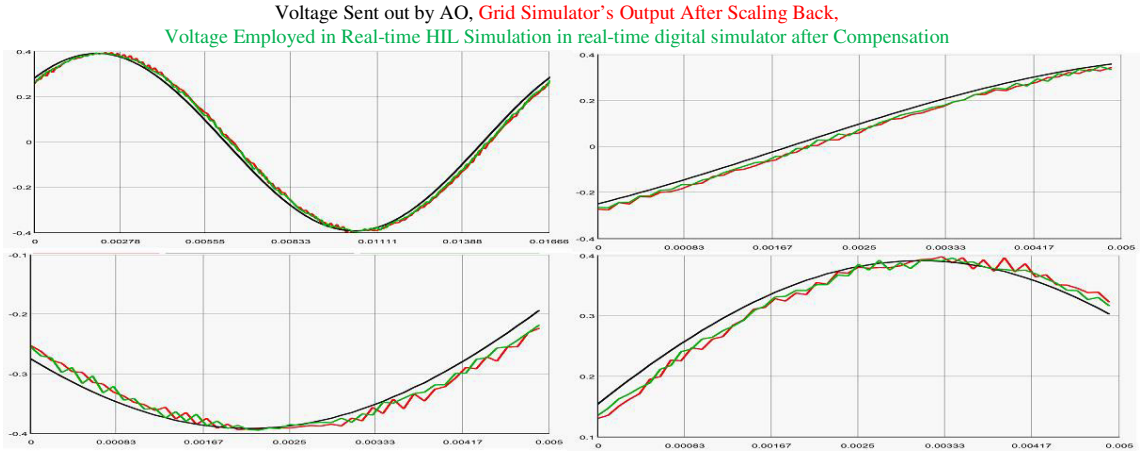


Fig. 8: Voltage employed in PHIL simulation; Black: voltage sent out by AO Card, Grid Simulator's output after scaling back, Green: voltage employed in real-time PHIL simulation in real-time digital simulator after compensation.

To test the funtionality of the proposed structure, the suggested compensated PHIL has been tested for a typical 15kW distrinbution PV inverter as a device under test. The single line diagram of the system id demonstrated in Fig. 9. The nominal voltage of different bus has been written on top of them. The PV inverter capacity is 15kW at 480V. The system has simulated for PHIL study under three different test cases. The first case is nominal operation (steady state power exchange). The second case is a capacitor switching event to test transients. The third case is a single-phase to ground (LG) fault, and the fourth case is a three phase (LLLG) fault. The test results are shown in Fig. 10, Fig. 11, Fig. 12, and Fig. 13, respectively.

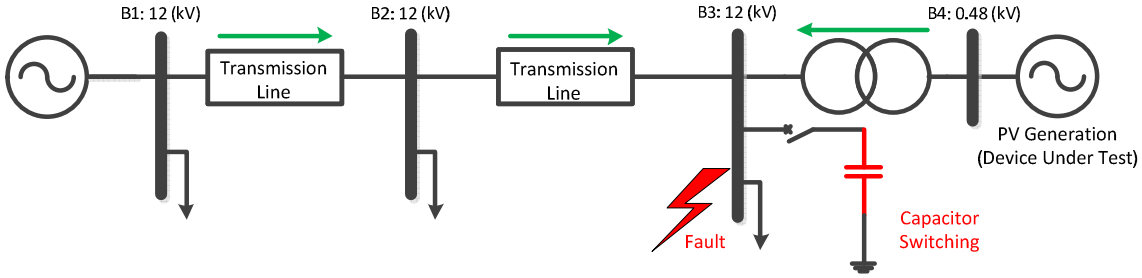
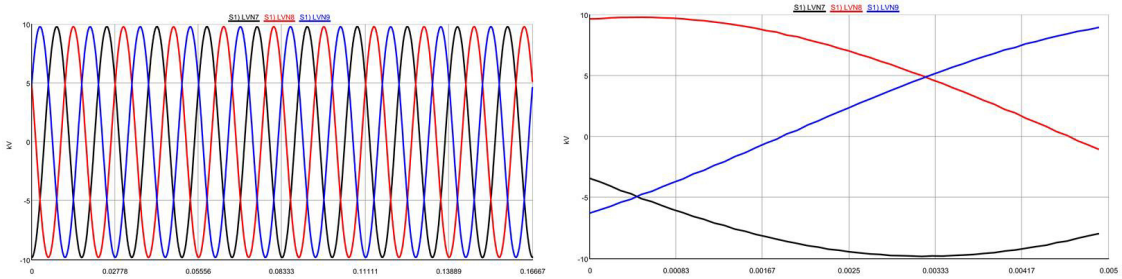
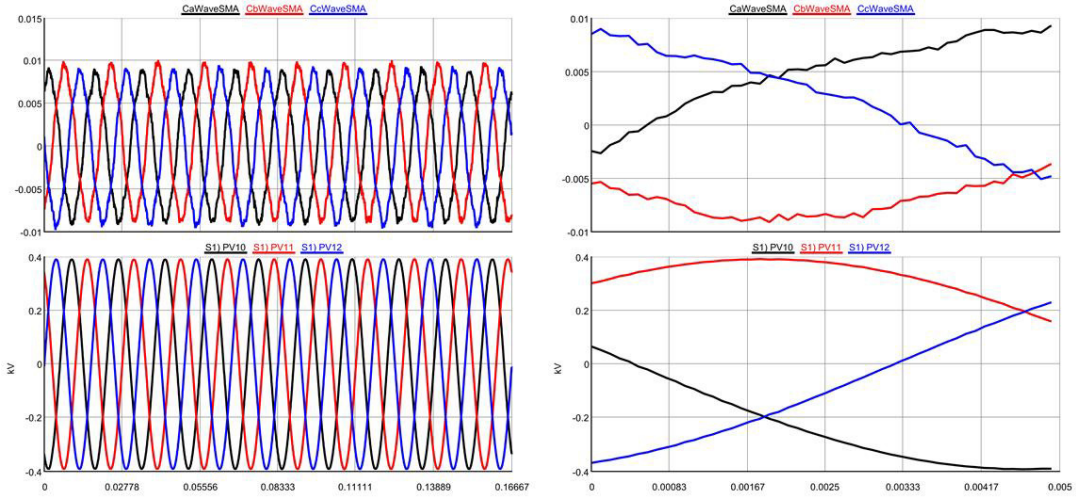


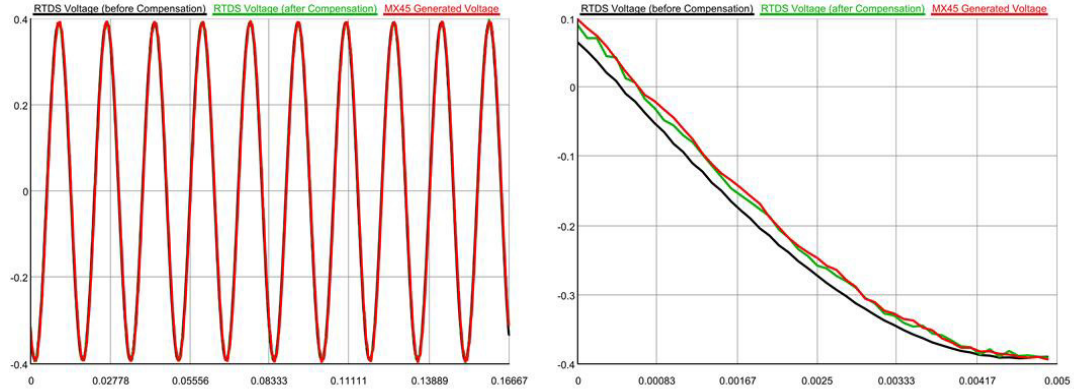
Fig. 9: Single-line diagram of the power system under study and device under test



Bus 3 Voltage (kV)

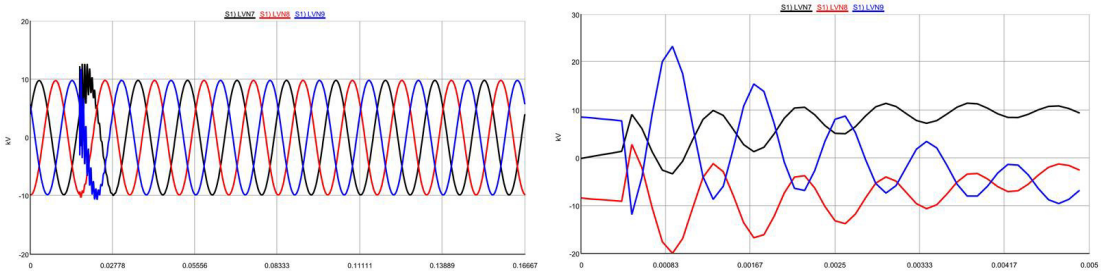


Bus 4; Top: Injected Current (kA), Bottom: Voltage (kV) at the Device under Test (DUT)

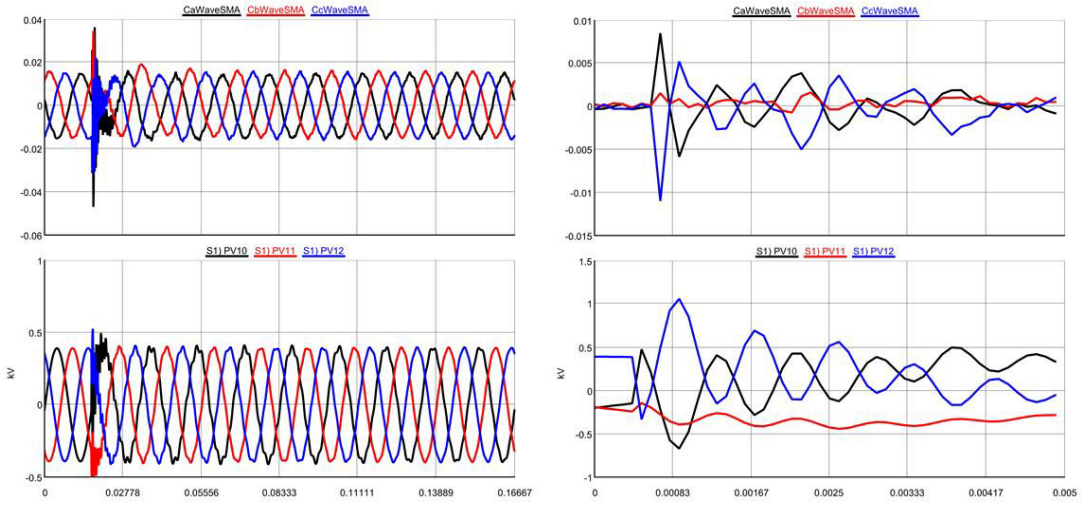


HIL Voltage (kV); black: simulated voltage in the real-time digital simulator before compensation, green: simulated voltage in the real-time digital simulator after compensation, red: generated voltage by grid simulator

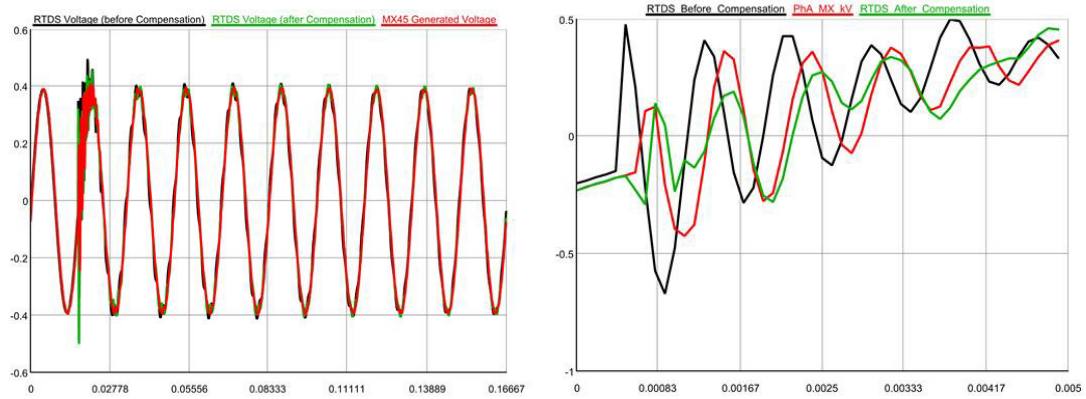
Fig. 10: PHIL Simulation for the case of normal operation



Bus 3 Voltage (kV)

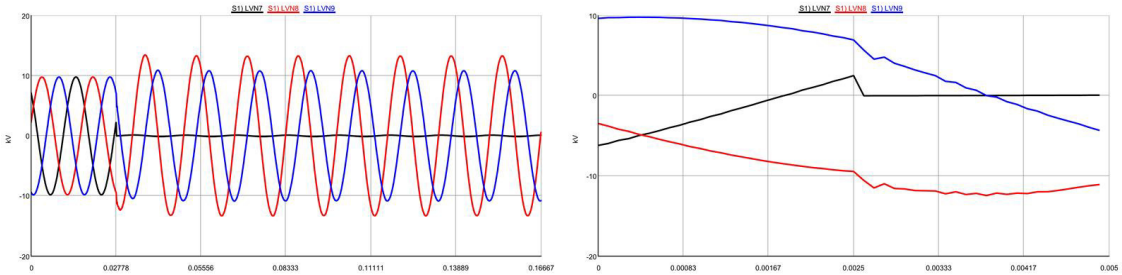


Bus 4; Top: Injected Current (kA), Bottom: Voltage (kV) at the Device under Test (DUT)

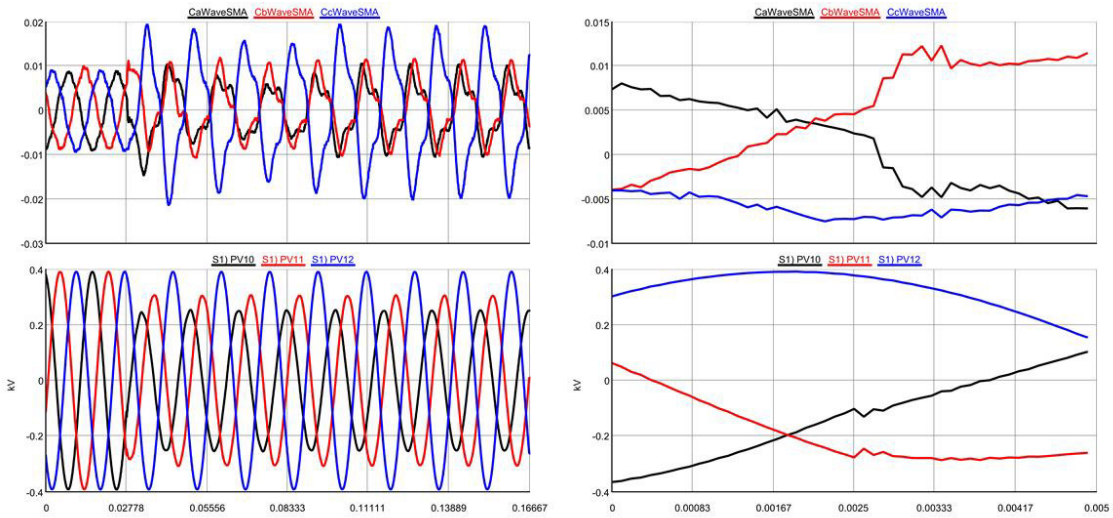


HIL Voltage (kV); black: simulated voltage in the real-time digital simulator before compensation, green: simulated voltage in the real-time digital simulator after compensation, red: generated voltage by grid simulator

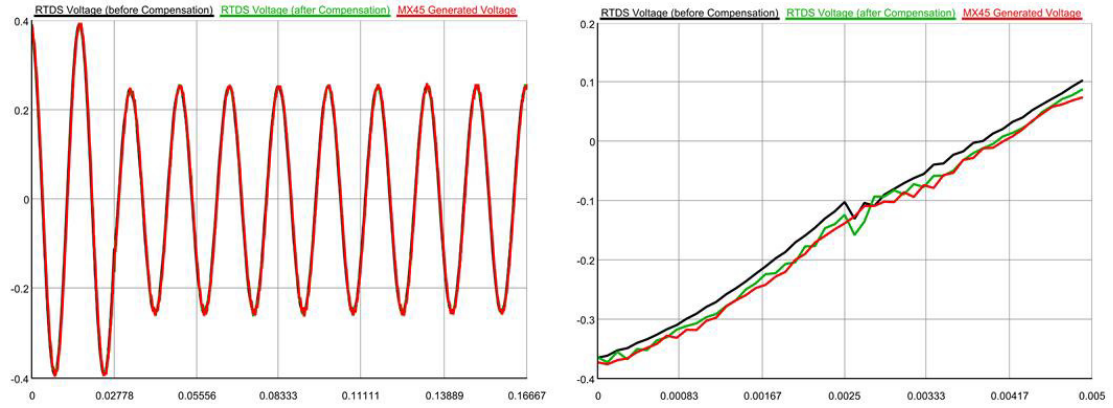
Fig. 11: PHIL Simulation for the case of a capacitor switching



Bus 3 Voltage (kV)

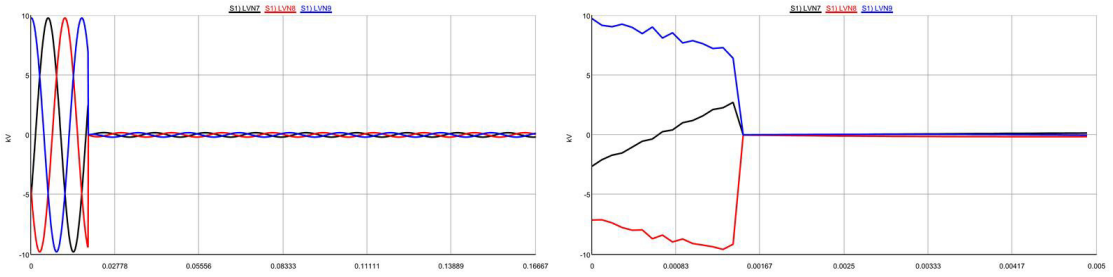


Bus 4; Top: Injected Current (kA), Bottom: Voltage (kV) at the Device under Test (DUT)

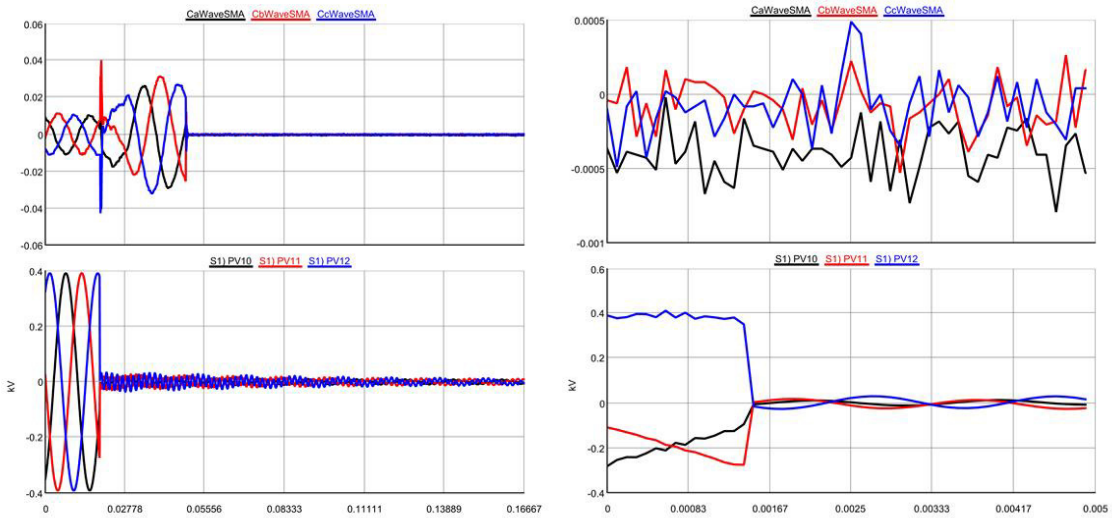


HIL Voltage (kV); black: simulated voltage in the real-time digital simulator before compensation, green: simulated voltage in the real-time digital simulator after compensation, red: generated voltage by grid simulator

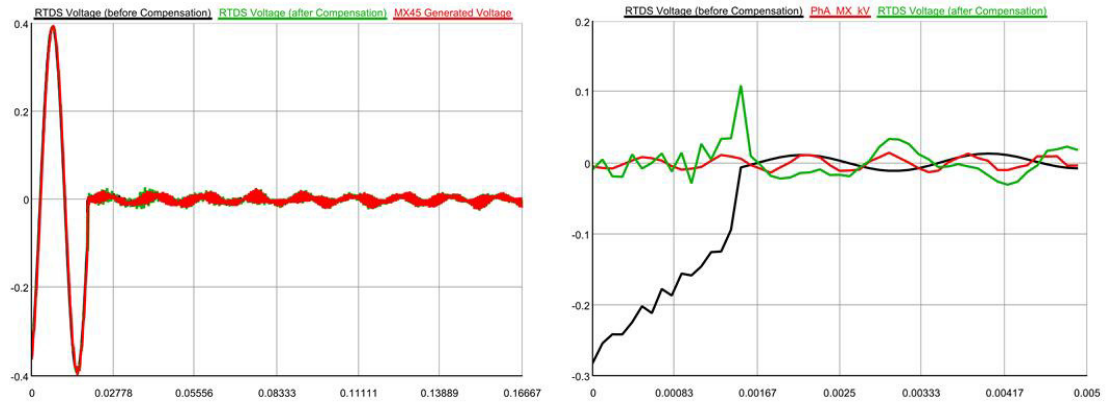
Fig. 12. PHIL Simulation for the case of a line to ground fault at 12 kV bus



Bus 3 Voltage (kV)



Bus 4; Top: Injected Current (kA), Bottom: Voltage (kV) at the Device under Test (DUT)



HIL Voltage (kV); black: simulated voltage in the real-time digital simulator before compensation, green: simulated voltage in the real-time digital simulator after compensation, red: generated voltage by grid simulator

Fig. 13: PHIL Simulation for the case of a three phase fault

As shown in Fig. 10 to Fig. 13, the proposed compensated PHIL simulation are very well matched with the generated grid simulator voltage and experimental results in all tests including normal operation test, switching test, single line to ground fault test, and three phase fault. In other words, the instant of occurring oscillations and their values are much matched for the compensated voltage in PHIL simulation and produced grid simulator voltage. It proves the functionality of the suggested PHIL enhance with voltage feedback.

CONCLUSIONS

PHIL is one of the recent industrial approaches for power systems and power electronics studies without applying load banks and physical medium/high voltage test feeders. The phase shift induced by grid simulators between its produced voltage and reference signal in real-time simulation results in instability, poor performance, and inaccurate results for PHIL simulations in steady-state and transient test cases, such as a short circuit fault, capacitor switching, and load rejection.

In this paper, phase shift induced by grid simulator in PHIL simulation was investigated, and it was proved that there is phase shift because of AI card, AO card, and grid simulator. Also, a compensation method in time domain was proposed for PHIL simulation to remove instability, poor performance,

and inaccurate results. The major benefits of proposed method is simplicity and employing time domain signal without finding and adding equivalent resistance and current in modelling, adding inductor in series with device under test, employing current filter, putting more burden on computation hardware, and applying PI controller in direct contrast of previous suggested methods.

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