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CIGRE US National Committee
2015 Grid of the Future Symposium

Analysis and Mitigation of Harmonic Currents and Instability due to Clustered Distributed Generation on the Low Voltage Network

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SUMMARY

Standards that DG PV inverters need to pass are tested under ideal conditions and do not guarantee satisfactory stability and harmonic performance on a realistic grid. Distortion and instability are compounded by increased clustering and crowding of granular DG's at a geographically small location. This paper proceeds with a detailed analysis stemming from the dynamics of the internal controls of each DG, demonstrating how clustering leads to emergence of aforementioned undesirable behaviour. A detailed model of the output impedance of each DG is derived and tied to the dynamical stability and steady state oscillatory response of the cluster accounting for the variance between a grid-tied or disconnected device. Furthermore the role of feedforward and the effect of its non-ideal nature is shown in detail. The relationship between stability and the ratio of the line impedance over DG total impedance is pointed out along with an analytical method of determining stability. Also amplification of centre of grid stiff voltage harmonics due voltage divider effect between line and transformer impedance and DG cluster output impedance is plotted. Finally the major mitigation strategies are explained, being the implementation of virtual RC damping and virtual negative capacitance within the DG internal control. A simulation based on an actual Low voltage network was built in Simulink and used to verify detrimental effects of DG clustering and effectiveness of mitigation techniques.

KEYWORDS

Harmonic distortion, stability, output impedance, negative capacitance, virtual damping, disturbance rejection.

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I. INTRODUCTION

Many offerings exist in the market for so called “micro-inverters” that individually couple with a single PV panel and tie into the low voltage grid. This granularity is attractive because it allows true staggered plug and play deployment and reduced installation costs. Naturally the bulk of embedded DG’s targeting utilities and residential markets is required to meet certain stringent specifications outlined in [1] and [2] aimed at preventing power quality degradation on the network. The aforementioned standards are partly concerned with limiting the harmonic currents and THD injected into the grid to within acceptable limits, however compliance tests to verify this are run with pure sine wave voltage sources far removed from realistic grid voltage waveforms observed in the field that do carry some harmonics. The rationalization of this testing procedure is the presumption of sufficiency for the DUT (device under test) to not add distortion under perfect conditions, while non-ideal conditions are not its responsibility. Grid connected inverters are in fact quite sensitive to grid voltage harmonics as will be quantitatively established in this paper. This sensitivity is compounded with increased penetration and is caused by residual DG output impedance that cannot be tuned out across the whole frequency range. An outline in general strokes of high DG penetration induced harmonic distortion is described in [3] and is essentially a lumped resonant elements model. This paper will focus on a detailed analysis of the root cause of those resonances in the dynamics of the inverter control.

II. ANALYSIS

A. *Output impedance of a single embedded generator*

The two stage inverter architecture is currently the most versatile in that it allows high fidelity output current forming in all 4 power quadrants, hence it can provide reactive power if required. Single stage designs will have simpler output impedance characteristics dominated by the passive filtering elements connecting the output terminals. In the two stage design the first stage appears as controlled load to the PV panel to steer it towards its maximum power point, dumping all harvested energy into the DC link reservoir capacitance. This capacitance needs to supply peak AC power at double the available PV power so must be sized accordingly. A properly sized DC link capacitor will keep its voltage higher than the peak voltage of the grid with small ripple, so that the PWM driven H-bridge can correctly shape the output current by balancing the voltage difference across the output inductance. Note that the time constant of the DC link voltage is a couple orders of magnitude larger than the much faster current shaping dynamics, even when the DC link capacitance is minimized for cost and reliability reasons, so it follows that the closed loop of the output stage will dominantly look like Fig 1. The controller G_c outputs a duty cycle which modulates the nominal DC link voltage to set the average voltage at one side of the filter inductance L_f, and is described by equation (1). It consists of an integrator with gain K_I to eliminate steady state errors (at dc only for at line frequency the gain is not infinite albeit high) and a phase lead compensator (simple pole ‘f_p’ and zero ‘f_z’ pair) to damp the marginal loop.

$$G_c(s) = \frac{K_I}{s} \frac{1 + {}^{s}\!/_{2\pi f_z}}{1 + {}^{s}\!/_{2\pi f_p}} \tag{1}$$

Utilizing superposition it can be shown that from the point of common coupling a single inverter looks like a current source that follows an internal reference signal i_{ref} up to the control bandwidth and an impedance in parallel. A circuit model of said impedance is derived (equations (2)-(4)) and consists of a series capacitor inductor pair and an RC mesh representing the damping effect of the compensator as shown in Fig 2. This impedance is designated Z_{ocr} (from Output Current Regulation) and combined with the passive output filter capacitance forms the full output impedance of a single inverter. Clearly the compensator’s effect is to dampen the resonance between the output filter inductance L_f and the control induced capacitance $C_{ocr.}$ T_{ocr} is the closed loop gain with V_{pcc} set to zero and is almost unity within the control bandwidth, while I_{ff} (s) is the feedforward current that is designed to ideally match the current into Z_{ocr} effectively removing it from the circuit so only C_f remains.

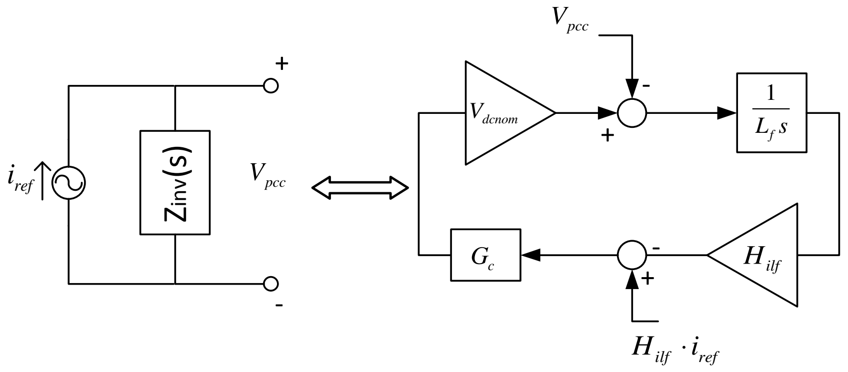


Fig 1 Equivalent circuit of inverter as seen from the point of common coupling (G_c: Controller, V_{dcnom}: DC link nominal operating voltage, V_{pcc}: voltage at point of common coupling, L_f: output inductance, H_{ilf}: current sense gain, i_{ref}: internal reference current)

$$R_{damp} = \frac{V_{dcnom}\left(f_p - f_z\right)K_I H_{ilf}}{2\pi f_p f_z} \tag{2}$$

$$C_{damp} = \frac{f_z}{V_{dcnom}\left(f_p - f_z\right)K_I H_{ilf}} \tag{3}$$

$$C_{ocr} = \frac{1}{V_{dcnom} K_I H_{ilf}} \tag{4}$$

The virtual C_{ocr} is much larger than the actual filter capacitance and dominates the impedance at low frequencies if no feedforward is implemented, as seen in the red plot of Fig 3. At high frequency the filter inductance L_f starts turning Z_{ocr} to the inductive side until its value gets high enough for C_f to dominate. Feedforward is simply implemented as direct sensing of the point of common coupling voltage and injecting it into the current control loop to cancel the effect of grid disturbances. Such a scheme is equivalent to multiplying V_{pcc} by a negative admittance equal to -1/Zocr, but due to limits on the sensing bandwidth and immunity to noise V_{pcc} cannot be perfectly sensed at all frequencies. Equation (5) models this by passing the voltage first through a filter H_{pcc} before injecting it into the loop.

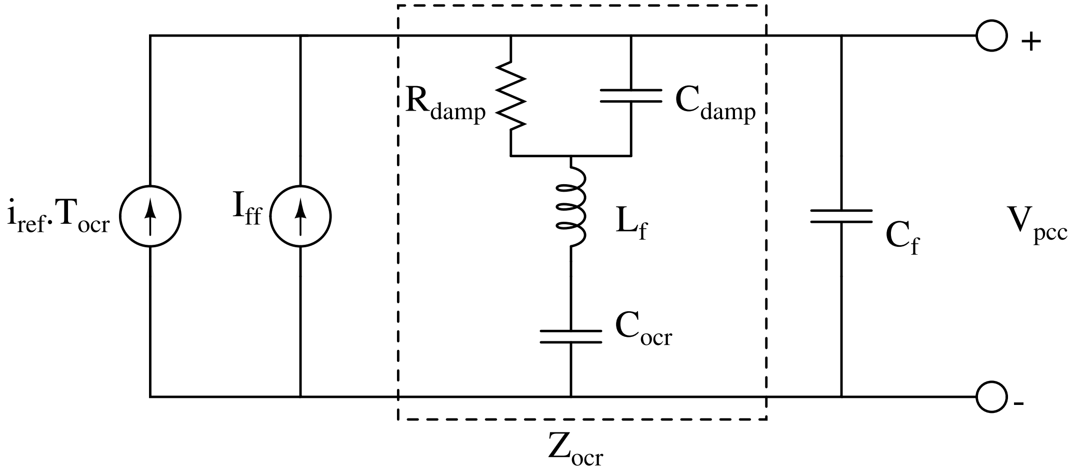


Fig 2 Component elements of output impedance of single inverter.

$$I_{ff}(s) = \frac{H_{pcc}(s)V_{pcc}(s)}{Z_{ocr}(s)} \tag{5}$$

The plots in Fig 3 are of equations (6) and (7) for sample parameters. Of note is the tenfold increase in output impedance at low frequency (blue plot) compared to no feedforward until the curves meet at high frequency.

$$Z_{inv}(s) = \frac{Z_{ocr}(s)}{1 + sC_f Z_{ocr}(s)} \tag{6}$$

$$Z_{inv,ff}(s) = \frac{Z_{ocr}(s)}{1 - H_{pcc}(s) + sC_f Z_{ocr}(s)} \tag{7}$$

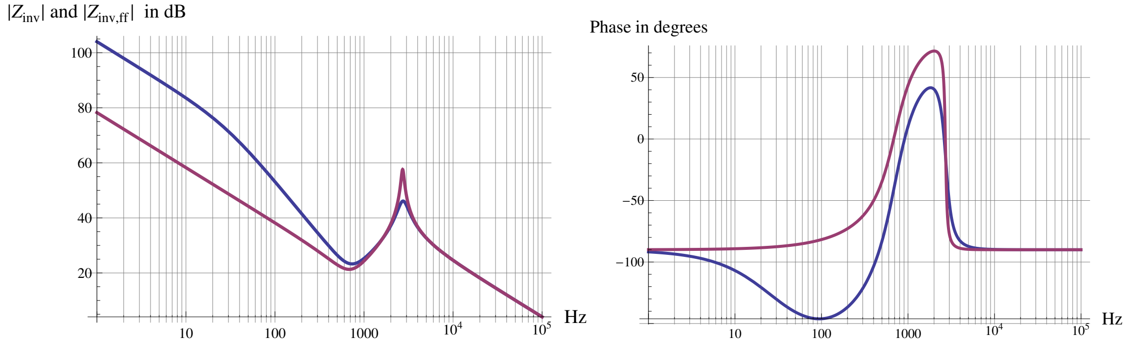


Fig 3 Output impedance of Single inverter with (blue) and without (pink) feedforward, including output filter capacitor (L_f: 4 mH, C_f: 1 µF, V_{dcnom}: 230V, H_{ilf}: 0.236, K_I: 1000, f_z: 500, f_p: 2000)

B. Output impedance of a cluster of embedded generators

When DGs are clustered with high density at the periphery of the low voltage network given that the output impedance of each DG is much higher than the interconnections impedances, it is quite accurate to assume that the equivalent output impedance is just a parallel connection of the lot. It has to be taken into account that a DG that is off will have a different output impedance than one that is on and actively pushing power into the grid. This difference presents itself in the form of the total DG impedance Z_{total} in equation (8) , where N_{total} is the total number of DGs connected to the network and N_{on} is the number of devices that are on at a particular instance in time.

$$Z_{total}(s) = \frac{1}{\dfrac{N_{on}}{Z_{inv,ff}(s)} + (N_{total} - N_{on})sC_f} \tag{8}$$

Right before sunrise the DGs are simply a passive capacitance connected to the grid, but as irradiance increases and more devices kick in output impedance starts to degrade at medium to high frequencies as shown in Fig 4. Harmonic currents induced by existing grid voltage harmonics then keep edging up until they peek with full participation of all DGs. Solely based on this effect it is possible for a hiccup scenario to arise where increased distortion will cause some devices to disconnect and connect cyclically.

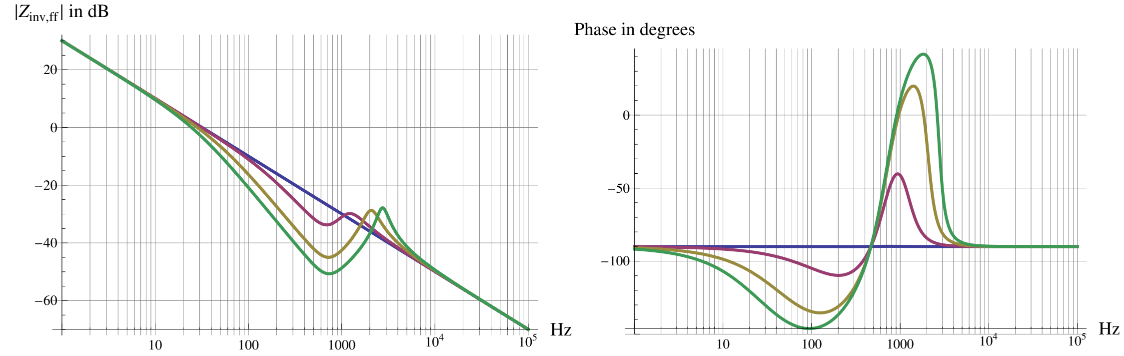


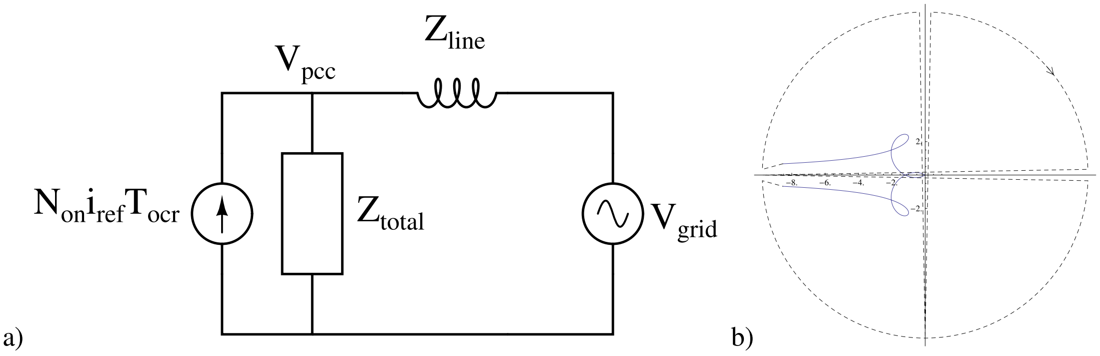
Fig 4 Output impedance of 5000 units as they come online (blue: 1 on, red: 500 on ,yellow: 2500 on , green: all units on)

C. Types of disturbance on low voltage network

The aggregate system of DGs when lumped as outlined in the previous section will interact with the centre of the grid through line impedance Z_{line} which is mostly inductive. It is an amalgam of conductor inductance and distribution transformer impedance which typically stands at 4 pu. Assuming a 500 KVA distribution transformer and a DG output filter inductance of 4mH yields a $|Z_{line}|$ that is 0.22% of that inductance. The lumped circuit model is shown in Fig 5a and shows that possible sources of disturbance for this system are either the current reference i_{ref} or the centre of grid voltage V_{grid}. A disturbance in the reference current is equivalent to noise or artefacts in the current sensing apparatus within the control bandwidth, while disturbances originating from the centre of the grid can be voltage harmonics or flicker. An important question to answer is if those disturbances when they occur tend to die away or build up until the trip limits of some or all of the DGs are reached. The transfer function of the line current and point of common coupling voltage from both i_{ref} and V_{grid} respectively has the same form and is readily given in equation(9).

$$\frac{i_{line}}{i_{ref}} = \frac{V_{pcc}}{V_{grid}} = \frac{1}{1+\dfrac{Z_{line}}{Z_{total}}} \tag{9}$$

The Nyquist criterion from classical control theory [4] is the easiest unambiguous (unlike the Bode technique) way to determine bounded input bounded output (BIBO) stability and the form of equation (9) indicates that the Z_{line}/Z_{total} transfer function is what must be fed into the criterion. A sample nyquist plot for a system with 800 DGs that is unstable is shown in Fig 5b, since the plot encircles the -1 point once and the open loop system has no poles on the right hand side. The chance of encircling -1 is very much dependent on the ratio $|Z_{line}/Z_{total}|$ which is the figure of merit for the stability of the system, the smaller the better.



a)

b)

Fig 5 a) Lumped model of DG interaction with centre of the grid b) Nyquist plot for 800 DGs on out of a total of 5000

Global stability is not the only characteristic of importance though. The system could be stable but still carry oscillatory disturbances that manifest as unacceptable harmonic distortion. The point of common coupling voltage might become taxed with high harmonics due to the voltage divider effect between the line impedance and the DGs. When most devices are off there is a sharp resonance between the passive output capacitance and the line, and as devices come online it tends to reduce in peak but shift towards lower frequencies were its effects are more pronounced (see Fig 6).

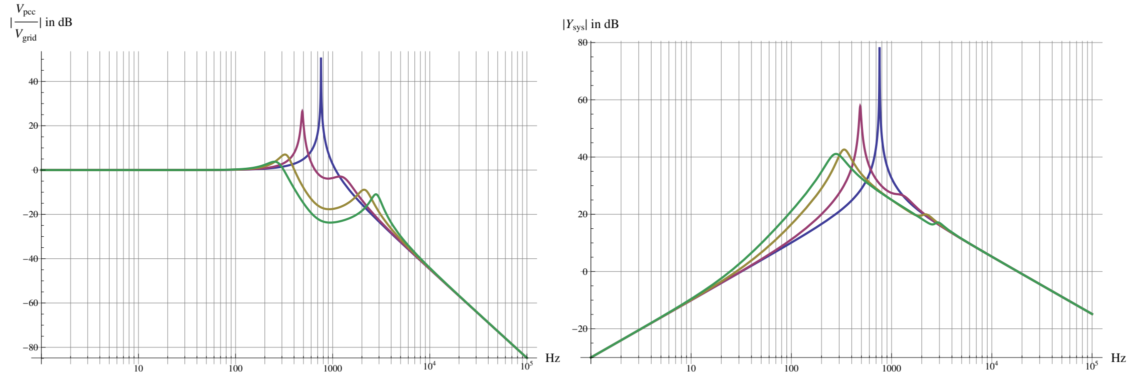


Fig 6 Gain from center of grid disturbance to point of common coupling voltage ($|V_{pcc}/V_{grid}|$) and line current ($|Y_{sys}|$) respectively.

Amplification of disturbance is much more prominent for the network current. The magnitude plot of the full system admittance $|Y_{sys}|$ demonstrates an 80 dB peak that drifts down in frequency as more DGs come online increasing harmonic currents up to the 10th, most severely around the 5th harmonic where there is a tenfold increase in distortion.

D. Mitigation

Mitigation of harmonic distortion can be carried out in a twofold manner based on the developed DG output impedance model. The foremost goal is to insure stability by providing extra damping and to reduce steady state oscillations due to stiff harmonics coming from the centre of the grid. Both can be achieved by implementing a virtual RC damping branch and a virtual negative capacitance respectively. Implementing negative capacitance is through filtering V_{pcc} and differentiating then scaling by $H_{ilf}C_{neg}$ before adding the result to the reference current of the OCR loop. Of course this negative capacitance only manifests within the bandwidth of the OCR control loop where is compensates for the base impedance consisting of the output filter capacitance (C_f) so raising the output impedance overall. It is important to note that too much negative capacitance can cause positive feedback and instability, and should always be tested against Nyquist criterion for equation (9).

A general rule of thumb is to apply enough negative capacitance to cancel out the output filter capacitance only and not the C_{ocr} and then to implement an RC damping branch with a corner frequency within the OCR bandwidth but above the fundamental frequency to load harmonic currents and diminish oscillations.

III. SIMULATION

A Simulink simulation was built based on a sample low voltage distribution network built by an actual Utility with the intention of distributing 708 DG's across said network (see Fig 7). This LV network was fed by a 6/0.23 KV distribution transformer with 6.5% impedance and X/R equal to 2, and copper wiring data and lengths was utilized to incorporate in the model all impedances between transformer and connection points (CP's) for the DGs which were rated 0.24 KVA each. The DGs were distributed evenly among the connection points. Fig 8a demonstrates that with no mitigation whatsoever the network cannot even accommodate a small number of DG's and exhibits severe instability at 24 connected. Negative capacitance raises the impedance enough to allow 177 DGs to be connected albeit with oscillations way beyond acceptable range (see Fig 8b). Finally the addition of damping allows all 708 DGs to be connected with adequate harmonics.

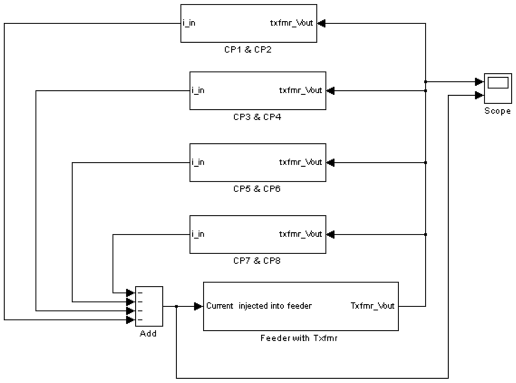
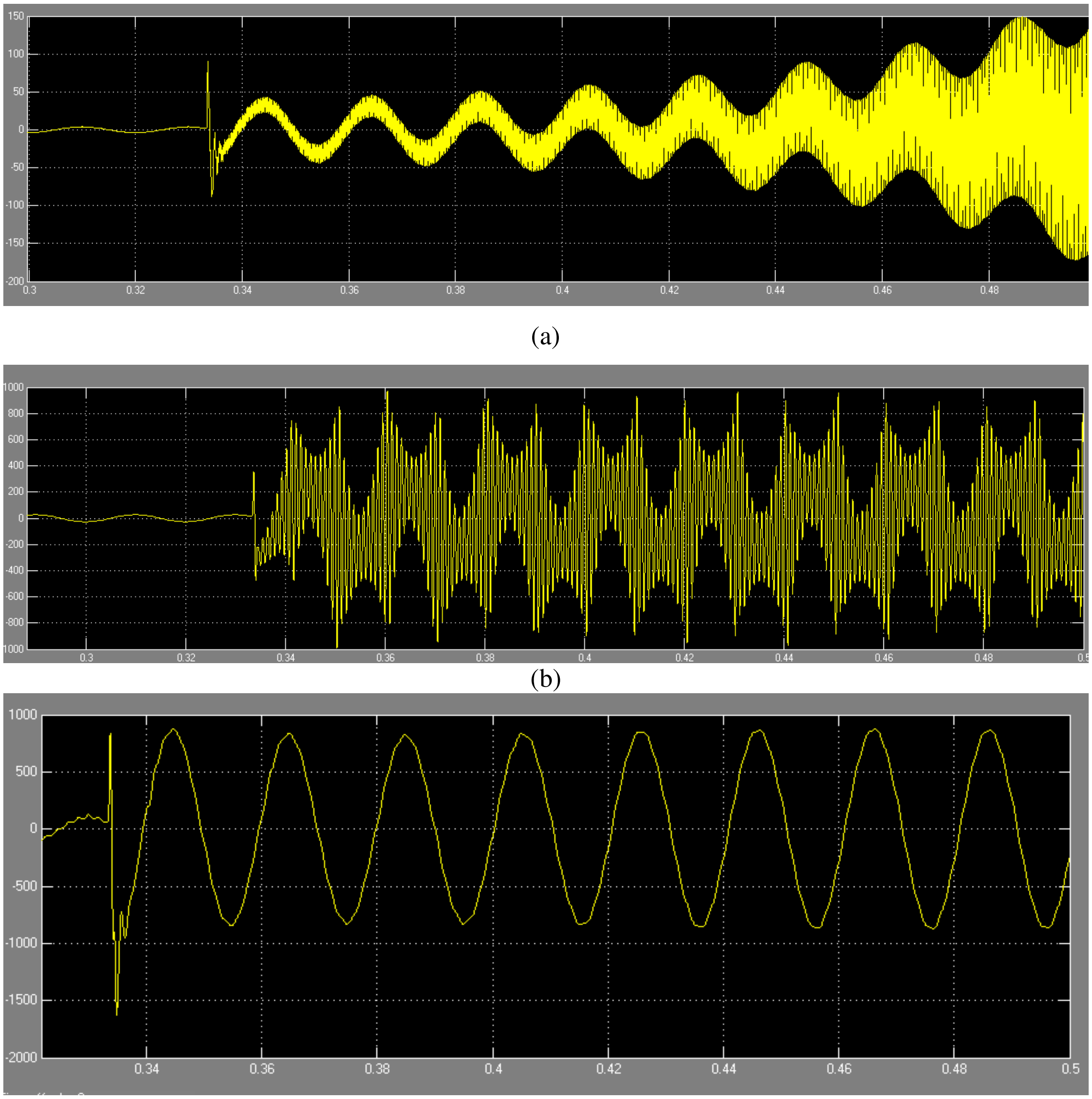


Fig 7 Simulation model of Sample feeder with distributed DG's



(a)

(b)

(c)

Fig 8 Total DG current for : (a) 24 DGs with no mitigation, (b) 177 DGs with negative capacitance, (c) 708 DGs with negative capacitance and damping

IV. CONCLUSIONS

A detailed analytic exposition was established in this paper for the harmonic distortion and instability issues encountered in clustering of distributed micro-generation at the "last-mile" low voltage network. This analysis was used to suggest mitigation techniques that were demonstrated to be effective in simulation of a sample network. The analysis and those mitigation methods were developed in the continuous domain but can be trivially extended to digitally controlled DGs. Microgeneration is gaining in traction due to its economic and ease of installation advantages at the low voltage network. Aforementioned harmonic distortion and instability issues due to DG increased penetration was reported in the literature and by some utilities, and as penetration keeps increasing the need for the detailed analysis presented in this paper cannot be understated.

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